


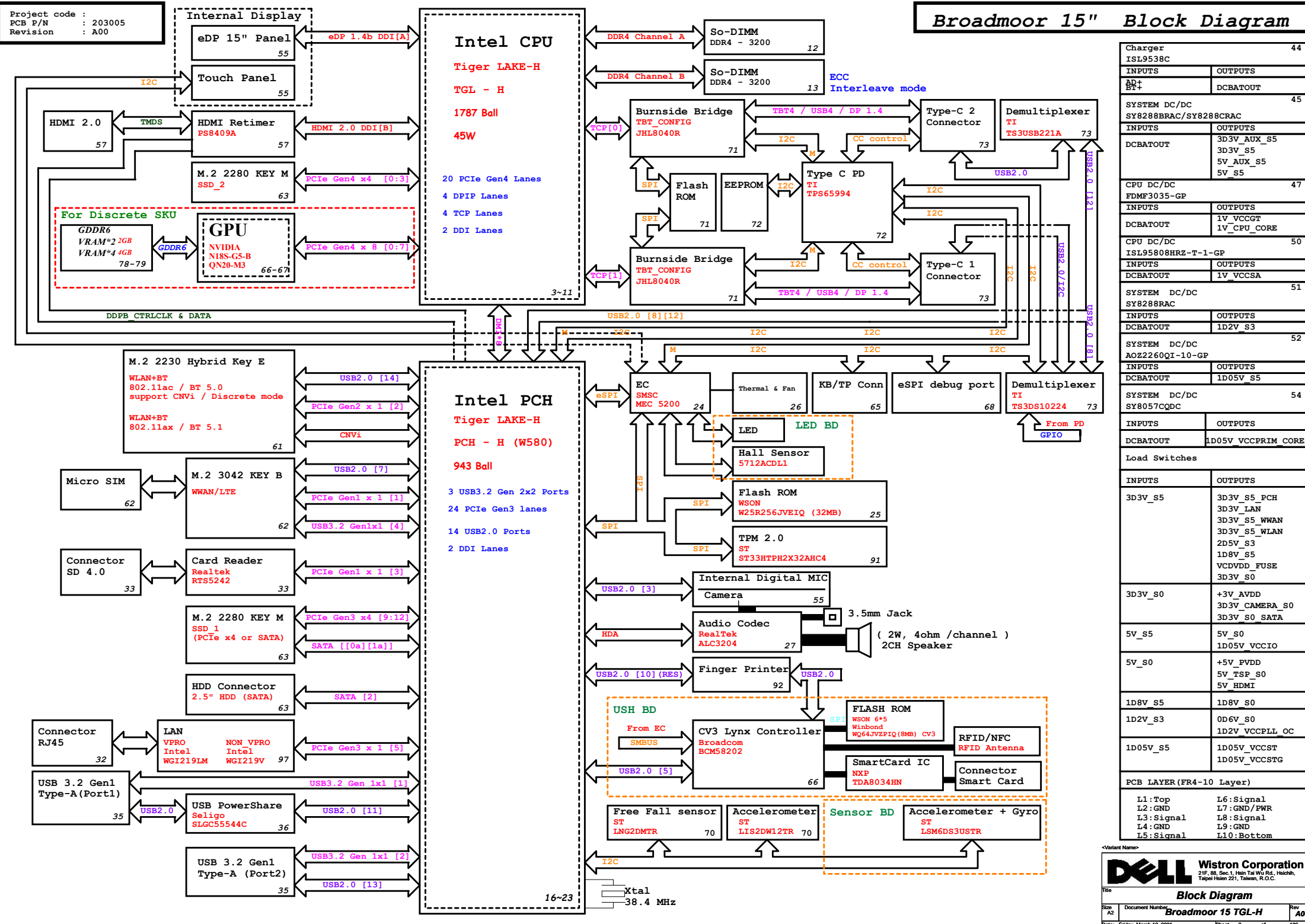
BROADMOOR 15 N18S-G5/QN20-M3 Schematics

Tiger Lake-H

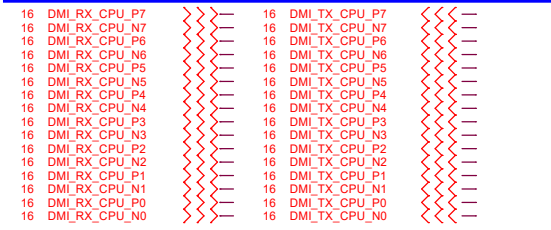
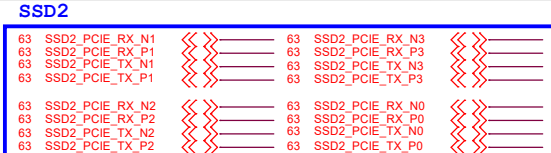
203005 REV: A00

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cover Page			
Size A4	Document Number Broadmoor 15 TGL-H		Rev A00
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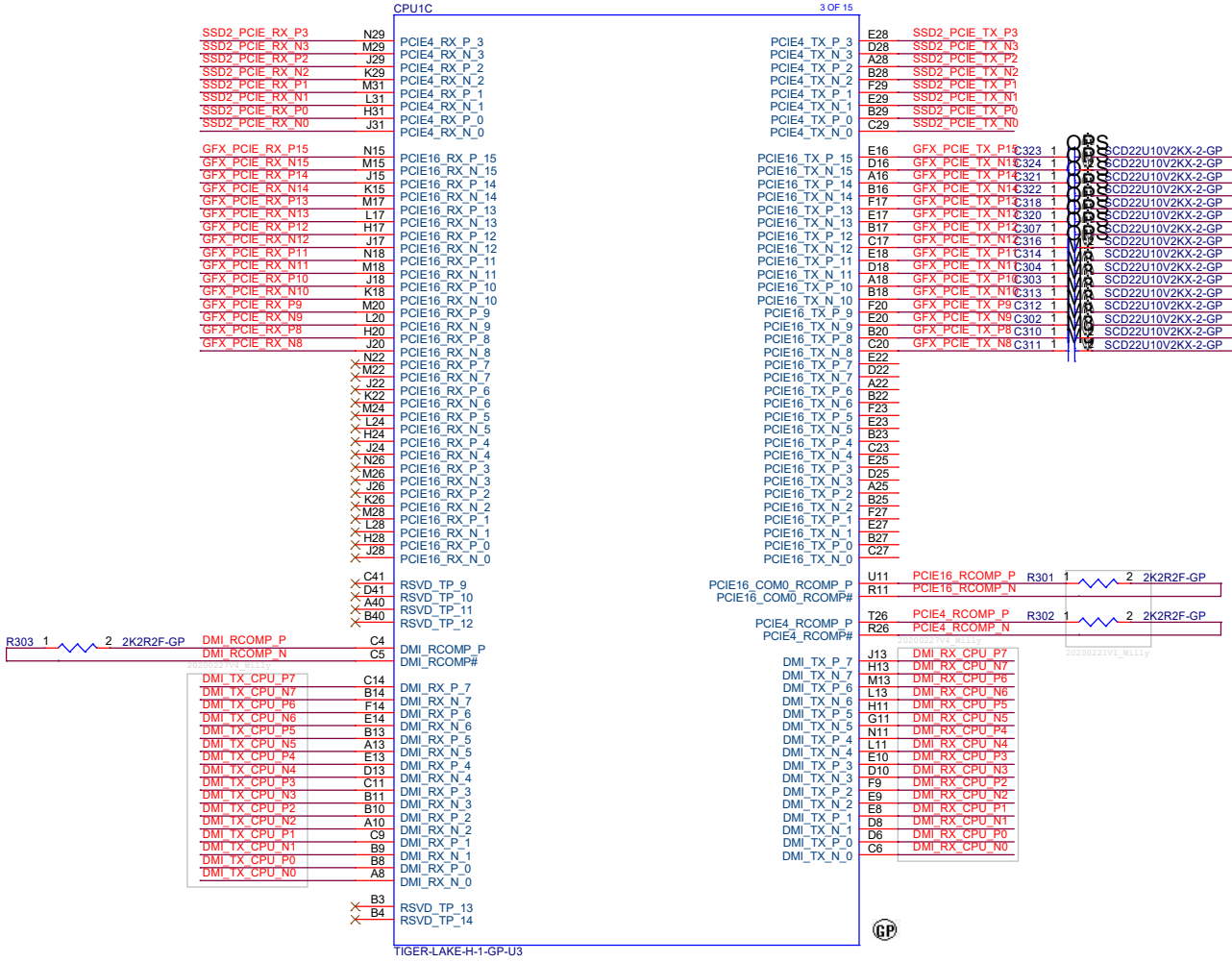
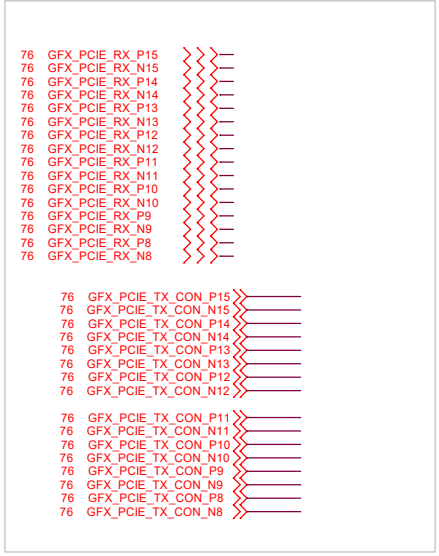


Charger		44
ISL9538C		
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	
SYSTEM DC/DC SY8288BRAC/SY8288CRAC		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_AUX_S5 5V_S5	
CPU DC/DC FDMF3035-GP		47
INPUTS	OUTPUTS	
DCBATOUT	1V_VCCGT 1V_CPU_CORE	
CPU DC/DC ISL95808HRZ-T-1-GP		50
INPUTS	OUTPUTS	
DCBATOUT	1V_VCCSA	
SYSTEM DC/DC SY8288RAC		51
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3	
SYSTEM DC/DC AOZ2260QI-10-GP		52
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S5	
SYSTEM DC/DC SY8057CQDC		54
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VCCPRIM_CORE	
Load Switches		
INPUTS	OUTPUTS	
3D3V_S5	3D3V_S5_PCH 3D3V_LAN 3D3V_S5_WWAN 3D3V_S5_WLAN 2D5V_S3 1D8V_S5 VCDVDD_FUSE 3D3V_S0	
3D3V_S0	+3V_AVDD 3D3V_CAMERA_S0 3D3V_S0_SATA	
5V_S5	5V_S0 1D05V_VCCIO	
5V_S0	+5V_FVDD 5V_TSP_S0 5V_HDMI	
1D8V_S5	1D8V_S0	
1D2V_S3	0D6V_S0 1D2V_VCCPLL_OC	
1D05V_S5	1D05V_VCCST 1D05V_VCCSTG	
PCB LAYER (FR4-10 Layer)		
L1:Top	L6:Signal	
L2:GND	L7:GND/PWR	
L3:Signal	L8:Signal	
L4:GND	L9:GND	
L5:Signal	L10:Bottom	



GFX_PCIE

20200313_Gen6



```

55 eDP_TX_CPU_N3  {{{{{{{
55 eDP_TX_CPU_P3  {{{{{{{
55 eDP_TX_CPU_N2  {{{{{{{
55 eDP_TX_CPU_P2  {{{{{{{
55 eDP_TX_CPU_N1  {{{{{{{
55 eDP_TX_CPU_P1  {{{{{{{
55 eDP_TX_CPU_N0  {{{{{{{
55 eDP_TX_CPU_P0  {{{{{{{
55 eDP_AUX_CPU_N  {{{{{{{
55 eDP_AUX_CPU_P  {{{{{{{

```

71	USB1_TCSS_TX_N0	↕	↕	—
71	USB1_TCSS_TX_P0	↕	↕	—
71	USB1_TCSS_TX_N1	↕	↕	—
71	USB1_TCSS_TX_P1	↕	↕	—
71	USB1_TCSS_RX_N0	↕	↕	—
71	USB1_TCSS_RX_P0	↕	↕	—
71	USB1_TCSS_RX_N1	↕	↕	—
71	USB1_TCSS_RX_P1	↕	↕	—
71	USB1_TCSS_AUX_N	↕	↕	—
71	USB1_TCSS_AUX_P	↕	↕	—

```

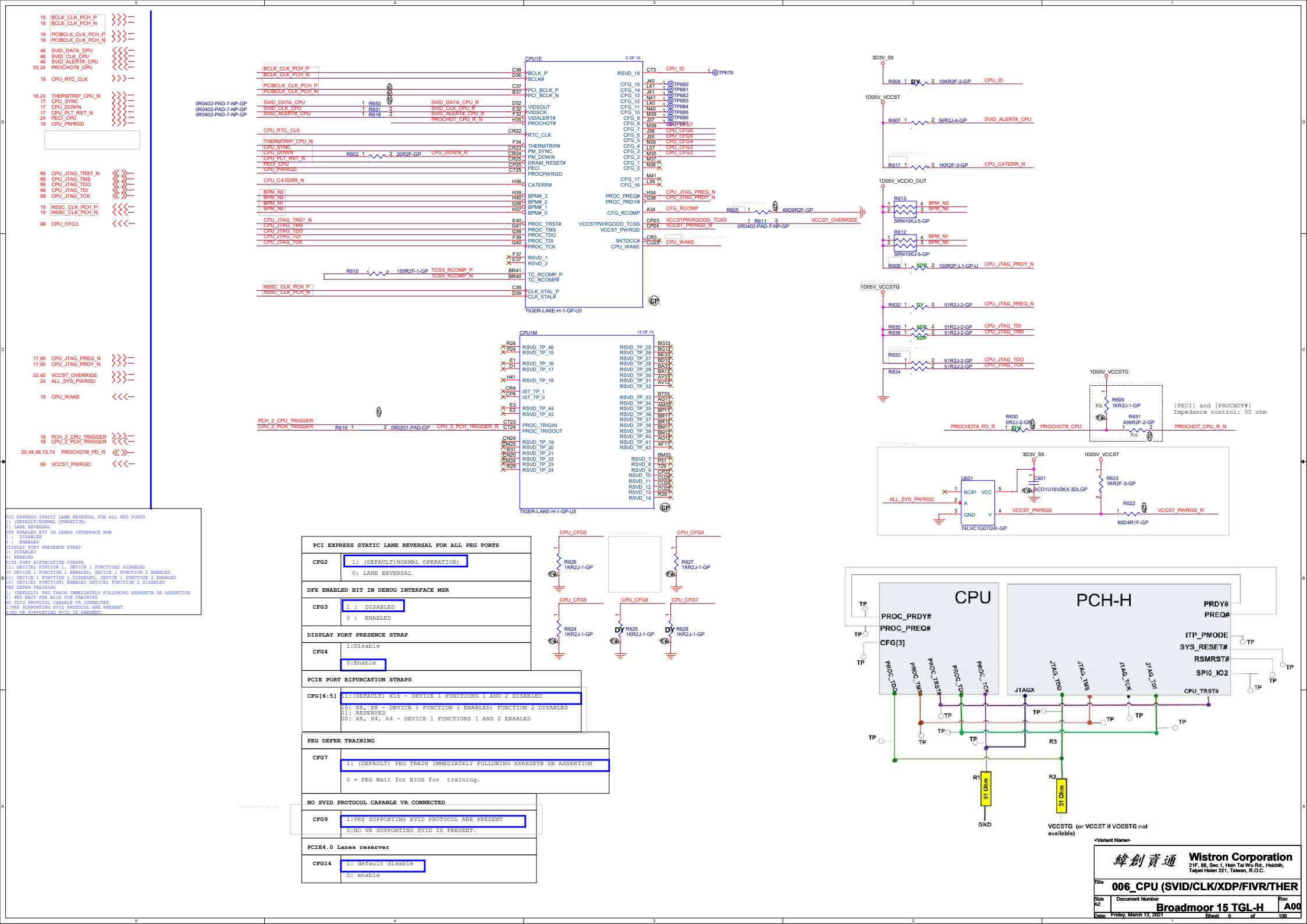
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71 USB2_TCSS_TX_P0  <<<<<  —
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71 USB2_TCSS_TX_P1  <<<<<  —
71 USB2_TCSS_RX_N0  <<<<<  —
71 USB2_TCSS_RX_P0  <<<<<  —
71 USB2_TCSS_RX_N1  <<<<<  —
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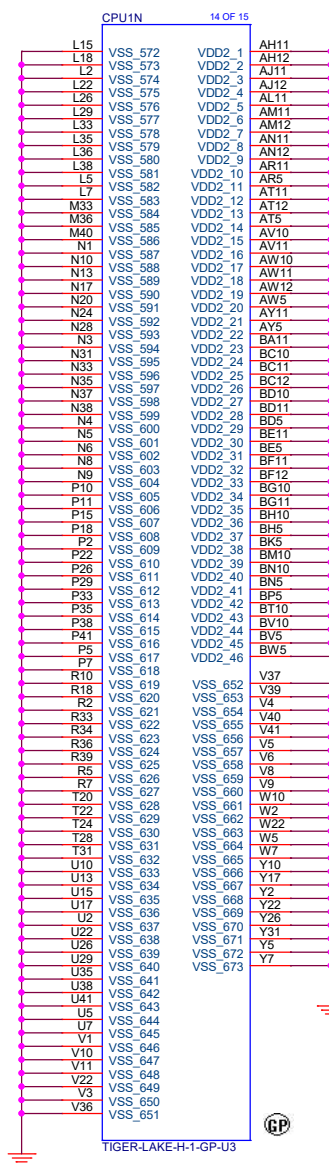
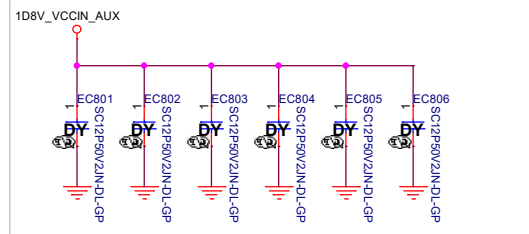
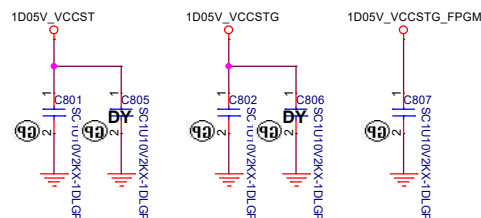
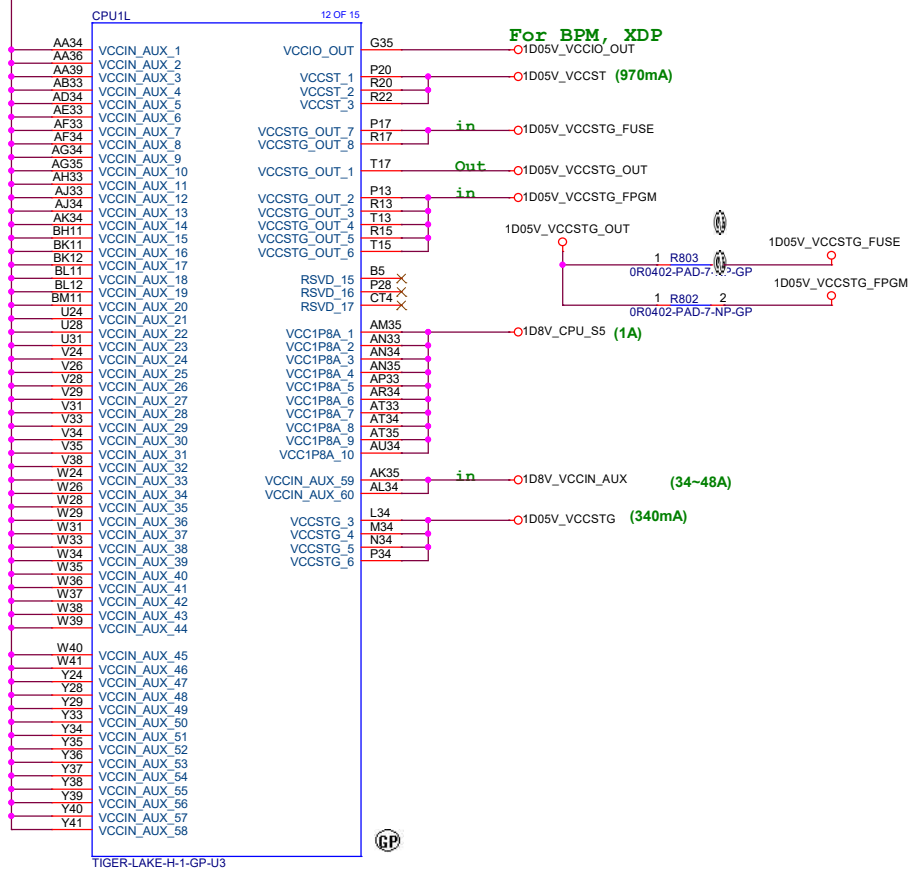
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0 AUD_AZACPU_SDI <<<—
0 AUD_AZACPU_SDO_R <<<—
0 AUD_AZACPU_SCLK <<<—
9 CPU_EAR <<<—







(22~42A)
1D8V_VCCIN_AUX

1D2V_S3 (4.3A)

1D8V_CPU_S5 (2A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

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1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

1D2V_S3 (4.3A)

Power Rail	Decap Placement	Form Factor	Value	Number
VDD2	Secondary Side	0603	22uF	2
		0402	10uF	1
		0402	Place Holder	2

<Variant Name>

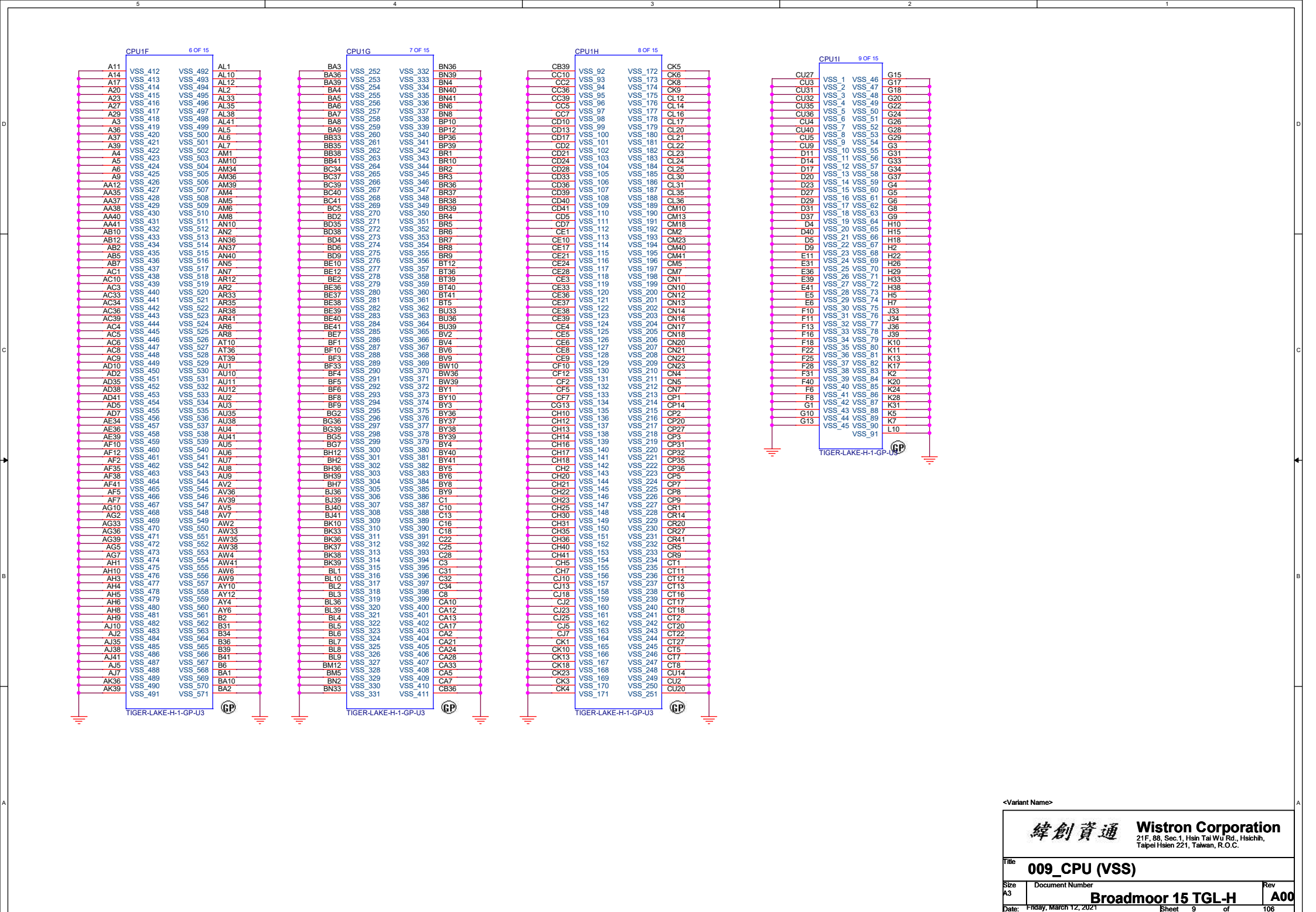
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 221, Taiwan, R.O.C.

Title 008_CPU (VCCIN_AUX/VCCST/VCCSTG

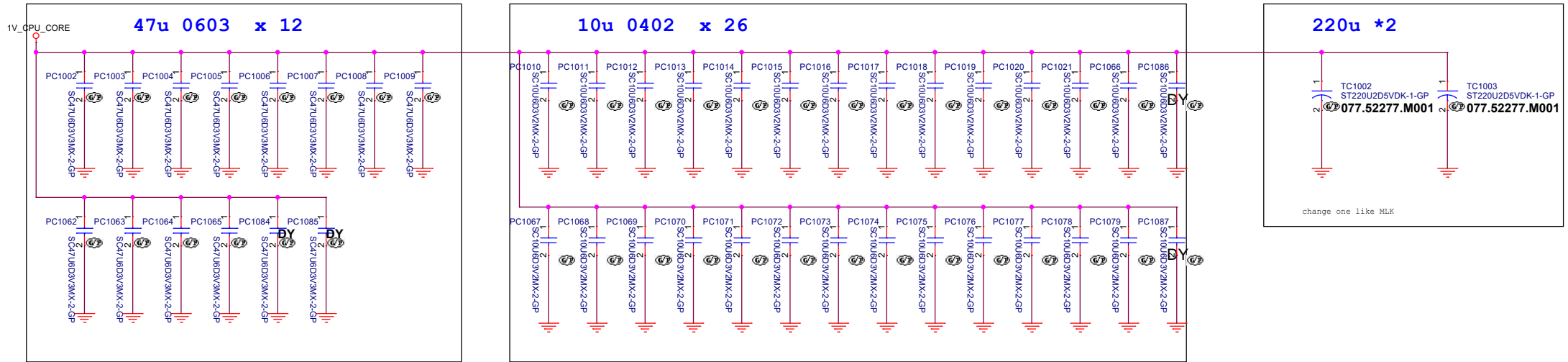
Size A3 Document Number Broadmoor 15 TGL-H Rev A00

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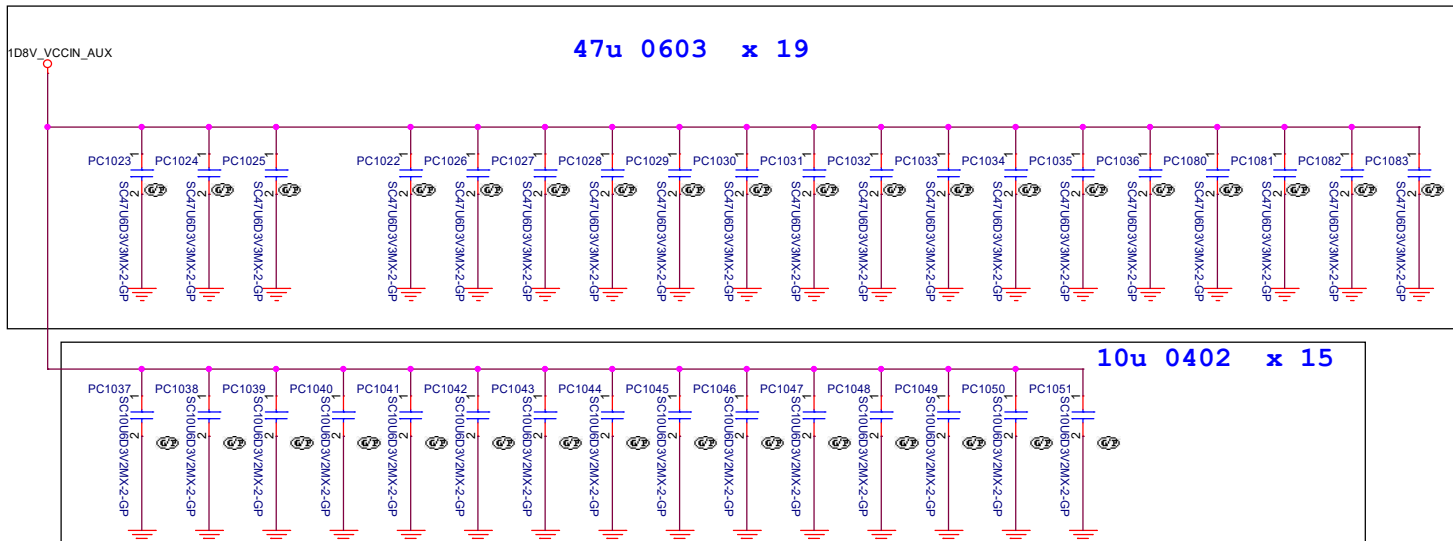


Main Func = CPU

1V_CPU_CORE (VCCIN)



VCCIN_AUX



Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN	Primary Side	7343	220uF (7mΩ ESR)	4
		7343	PlaceHolder	2
	Secondary Side	0603	47uF	10
		0603	PlaceHolder	2
		0402	10uF	25
		0402	PlaceHolder	2

Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX	CPU Primary Side	7343	330uF	2
		0603	47uF	4
	CPU Secondary side	0402	10uF	6
		0603	47uF	8
	PCH Primary Side	0603	47uF	5
		0402	10uF	4

<Variant Name>



Title			CPU (CORE Power Cap1)	
Size	Document Number	Broadmoor 15 TGL-H		Rev
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Date: Thursday, March 18, 2021		Sheet 10 of 106		

18.68 SPI_SI_CPU <<<-
18.68 SPI_WP_CPU <<>-
18.68 SPI_HOLD_CPU <<>-
21 HDA_SDOUT <<<-
21.61 CNV_RGI_DT >>>-
21 JTAG_ODT_EN <<<-
20.71 TBT_LSX0_RXD >>>-
20.71 TBT_LSX1_RXD <<<-
20.99 DBG_FMODE <<>-
21.61 CNV_BRI_DT <<<-
16.71 PCH_TBT_PERST# >>>-
21 TPM_IDENTIFY <<<-
20.24.27 SPKR <<<-
21 PEG_CFG_SEL <<<-
20 PCH_SMB_ALERT_N <<<-

GPIO	GPP_C5 eSPI Disable	SPIO_MOSI Reserved	GPP_H15 JTAG ODT Disable	GPP_J2 XTAL Freq Selection	SPI_IO_2 SPI_WP_CPU	GPP_R2 / HDA_SDO Flash Security Override	GPP_J4 / CNV_RGI_DT M.2 CNV1 Debug Mode Select	GPP_E6/SATA_DEVSLP2
Schematic								
High	Disable eSPI.	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Disable Flash Descriptor Security	INTEGRATED CNVI DISABLE	High for ST Micro
Low	Enable eSPI =default=	Reserved	JTAG ODT is disabled	38.4 MHz =default=	Reserved	Enable Flash Descriptor security measures	INTEGRATED CNVI ENABLE	Low for Nuvoton.
GPIO	GPP_G13 TBT_LSX0_VCC config	GPP_G15 TBT_LSX1_VCC config	GPP_G14 TBT_LSX2_VCC config	GPP_G11 TBT_LSX3_VCC config	SPI_IO_3 SPI_HOLD_CPU	DBG_FMODE	GPP_B18 No Reboot	GPD_7 Reserved
Schematic								
High	DDP1 I2C/TBT_LSX0/BSSB_LSO pins at 3.3V	DDP2 I2C/TBT_LSX1/BSSB_LSO pins at 3.3V	3.3V	3.3V	Reserved	DPXTESTMODE DISABLED (DEFAULT)	Enable "No Reboot" mode	Reserved
Low	DDP1 I2C/TBT_LSX0/BSSB_LSO pins at 1.8V	DDP2 I2C/TBT_LSX1/BSSB_LSO pins at 1.8V	1.8V	1.8V	Reserved	DPXTESTMODE ENABLED	Disable "No Reboot" mode	Reserved
GPIO	GPP_B14/SPKR	GPP_K4						
Schematic								
High	3.3V							
Low	1.8V							
								XTAL INPUT MODE HIGH : XTAL INPUT IS SINGLE ENDED LOW : XTAL IS ATTACHED

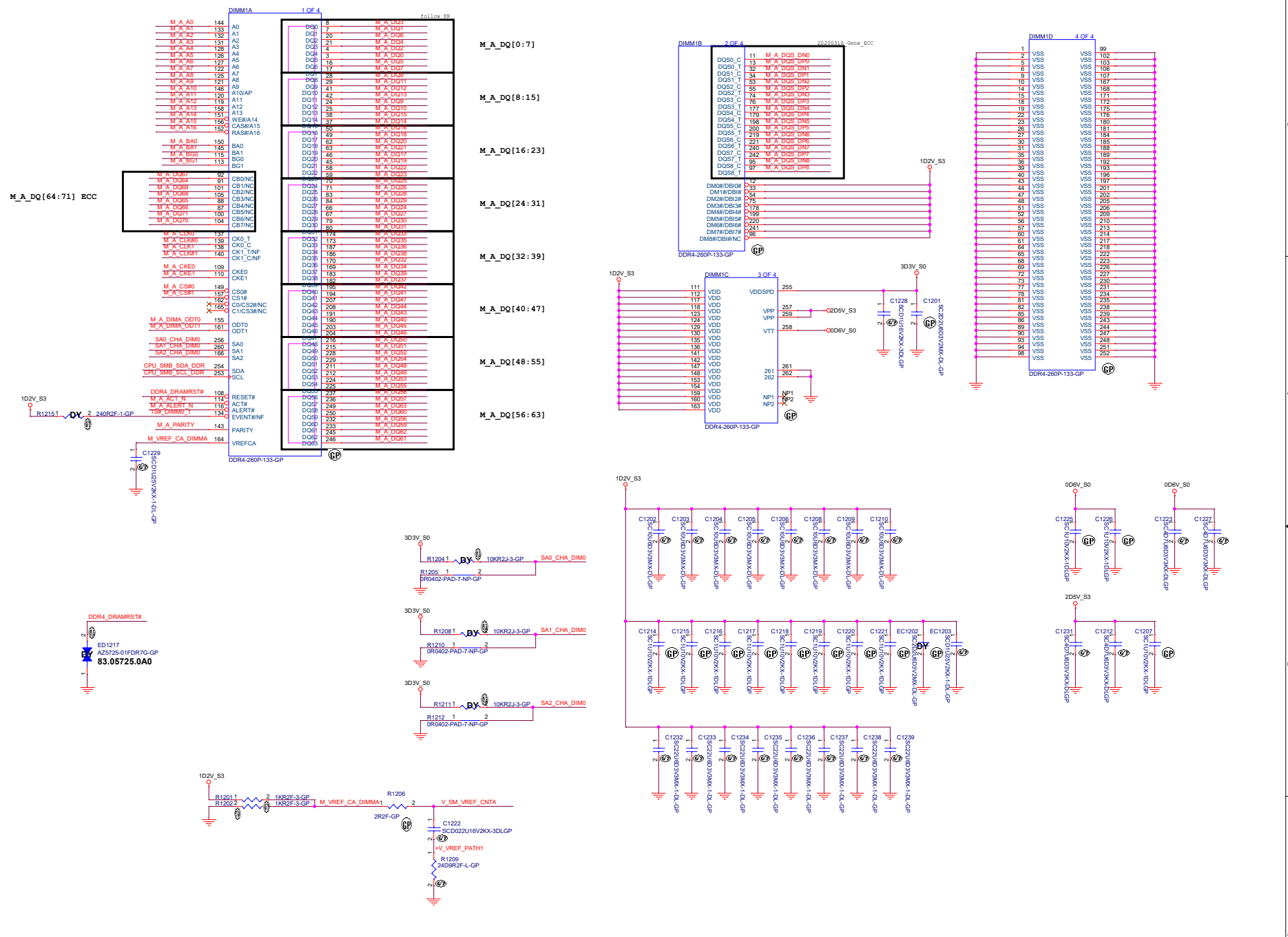
Original Ref.

GPP_C5	SPIO_MOSI	GPP_H15 / SML3ALERT#	GPP_J2/ CNV_BRI_DT	SPIO_IO2	GPP_R2 / HDA_SDO	GPP_J4/ CNV_RGI_DT	GPP_G13/ TBT_LSX0_VCC config	GPP_G15/ TBT_LSX1_VCC config	GPP_G9/ TBT_LSX2_VCC config
ESPI ESPI : ESPI IS DISABLED High : ESPI IS Enabled Weak INTERNAL PD	External pull-up is required. Recommended 4.7 kohm pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	JTAG ODT DISABLE HIGH : JTAG ODT DISABLED LOW : JTAG ODT ENABLED	XTAL SELECT-1 HIGH : JTAG ODT DISABLED LOW : JTAG ODT ENABLED	External pull-up is required. Recommended 100K if pulled up to 3.3V or 50K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.		This strap does not have an internal pull-up or pull-down. A weak internal pull-up is required. (x) = Integrated CNVI enabled (o) = Integrated CNVI disabled Note: When a BP comparison chip is connected to the PCH CNV1 interface, the device internal pull-down resistor will pull the strap low to enable CNVI interface.			
GPP_G11/ TBT_LSX3_VCC config	SPIO_IO3	DBG_FMODE	GPP_B18/ GSPT0_MOSI	GPD7	GPP_B14 / SPKR	GPP_C2/ SMBALERT#	GPP_B23/ SML1ALERT#	GPP_H12/ SML2ALERT#	GPP_B22/ GSPT1_MOSI
	External pull-up is required. Recommended 100K if pulled up to 3.3V or 50K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	This strap has a 20 kohm + 30% internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-up is disabled after RSPMST# de-asserts. 2. This signal is in the primary well.	No REBOOT HIGH : NO REBOOT LOW : REBOOT ENABLED Weak INTERNAL PD	This strap has a 20 kohm + 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSPMST# de-asserts. 2. This signal is in the GSN well.		This strap has a 20 kohm + 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after RSPMST# de-asserts. 2. This signal is in the primary well.			

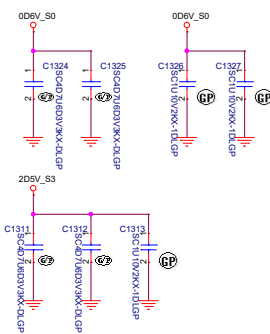
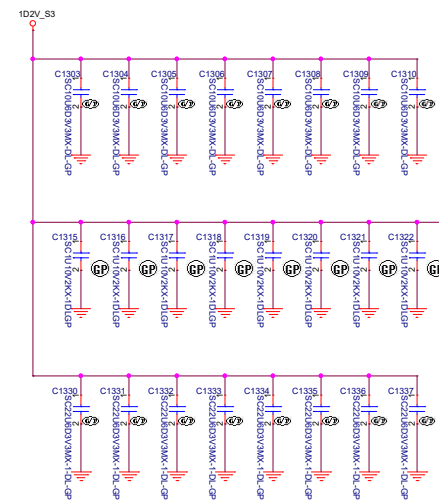
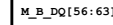
<Variant Name>

緯創實通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Main Func = MEMORY



```
12,13,20,70,96 CPU_SMB_SCL_DDR >>>
12,13,20,70,96 CPU_SMB_SDA_DDR >>>
```



5	4	3	2	1
D				D
C				C
B				B
A				A

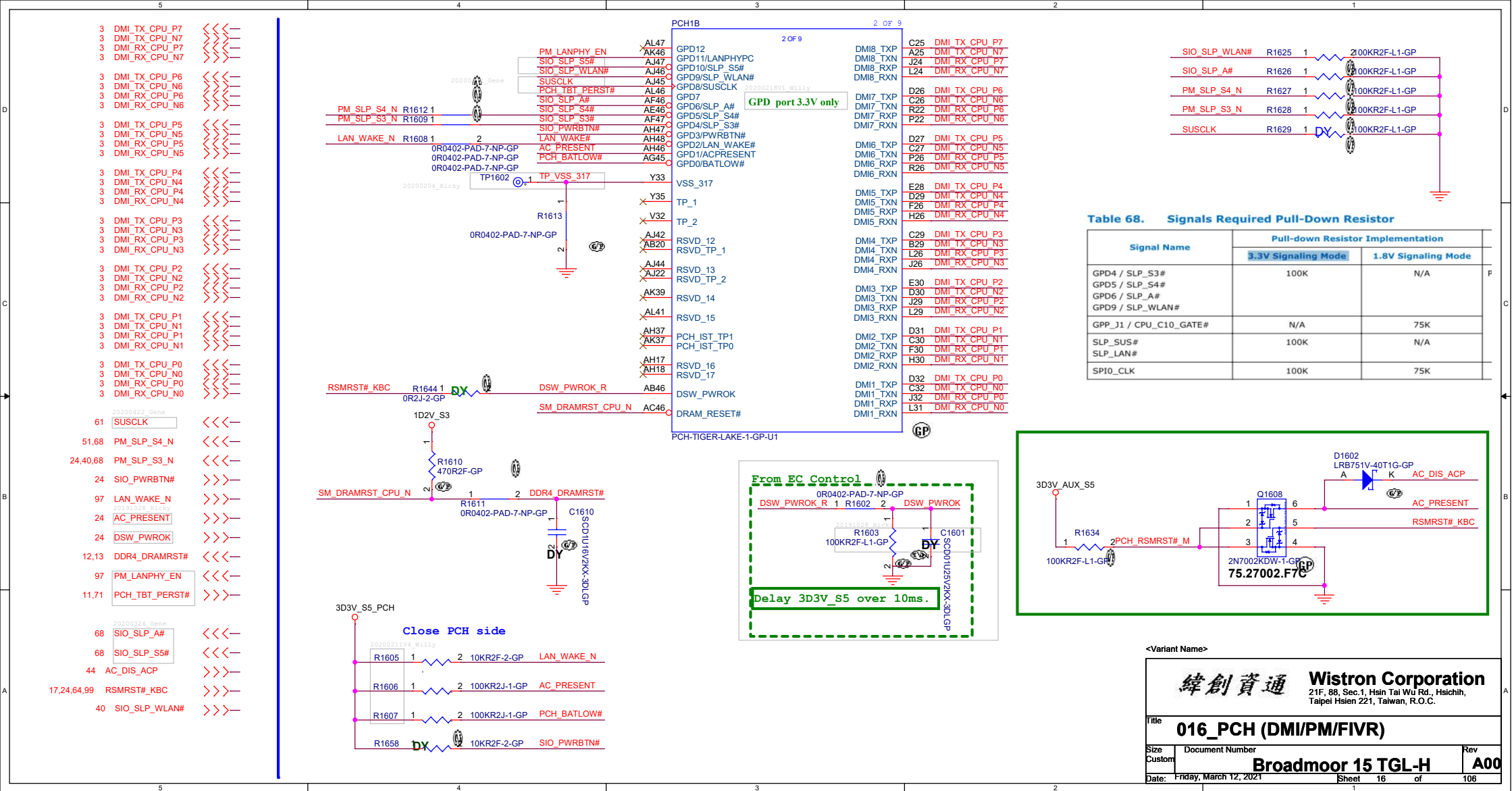
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<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title014_DDR (RSVD) (DDR4-CHA1)		
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5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title015_DDR (RSVD) (DDR4-CHB1)		
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WLAN

61 WLAN_PCIE_TX_P <<<-
61 WLAN_PCIE_TX_N >>>-
61 WLAN_PCIE_RX_P <<<-
61 WLAN_PCIE_RX_N >>>-

SSD1

63 SSD_PCIE_RX_N1 <<<-
63 SSD_PCIE_RX_P1 >>>-
63 SSD_PCIE_TX_N1 <<<-
63 SSD_PCIE_TX_P1 >>>-

63 SSD_PCIE_RX_N2 <<<-
63 SSD_PCIE_RX_P2 >>>-
63 SSD_PCIE_TX_N2 <<<-
63 SSD_PCIE_TX_P2 >>>-

63 SSD_PCIE_RX_N3 <<<-
63 SSD_PCIE_RX_P3 >>>-
63 SSD_PCIE_TX_N3 <<<-
63 SSD_PCIE_TX_P3 >>>-

63 SSD_SATA_RX_N <<<-
63 SSD_SATA_RX_P >>>-
63 SSD_SATA_TX_N <<<-
63 SSD_SATA_TX_P >>>-

LAN

97 LAN_PCIE_TX_P <<<-
97 LAN_PCIE_TX_N >>>-
97 LAN_PCIE_RX_P <<<-
97 LAN_PCIE_RX_N >>>-

6.99 CPU_JTAG_PRDY_N <<<-
6.99 CPU_JTAG_FREQ_N <<<-

6 CPU_SYNC <<<-
6 CPU_DOWN <<<-

6 CPU_PLT_RST_N <<<-

24 PCH_PCH <<<-

40.44 PCH_PWROK >>>-

16.24.64.99 RSMRST#_KBC <<<-

2020021703_M111g

2020021893_M111g

24 RTORST_ON <<<-

68 RTC_RST_N <<<-

WWAN

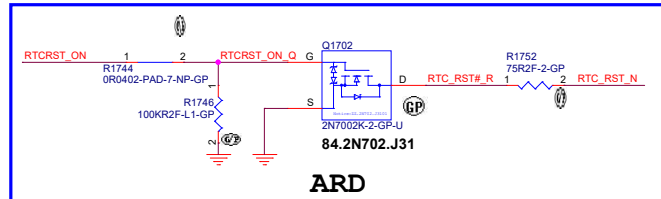
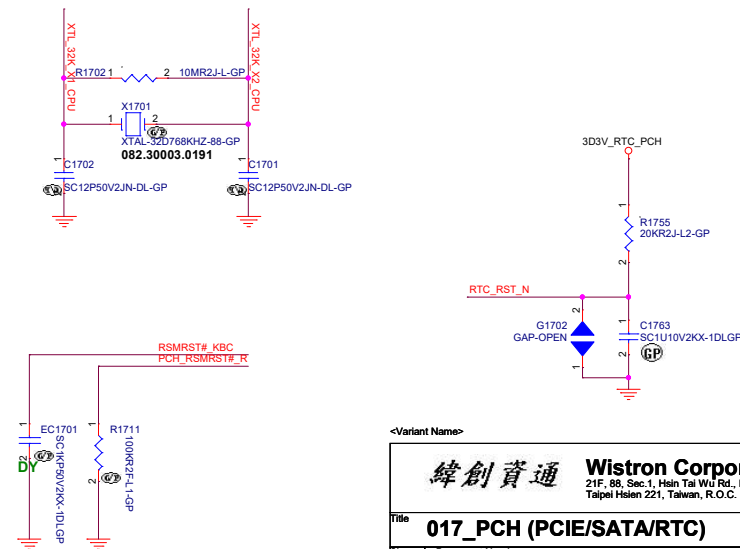
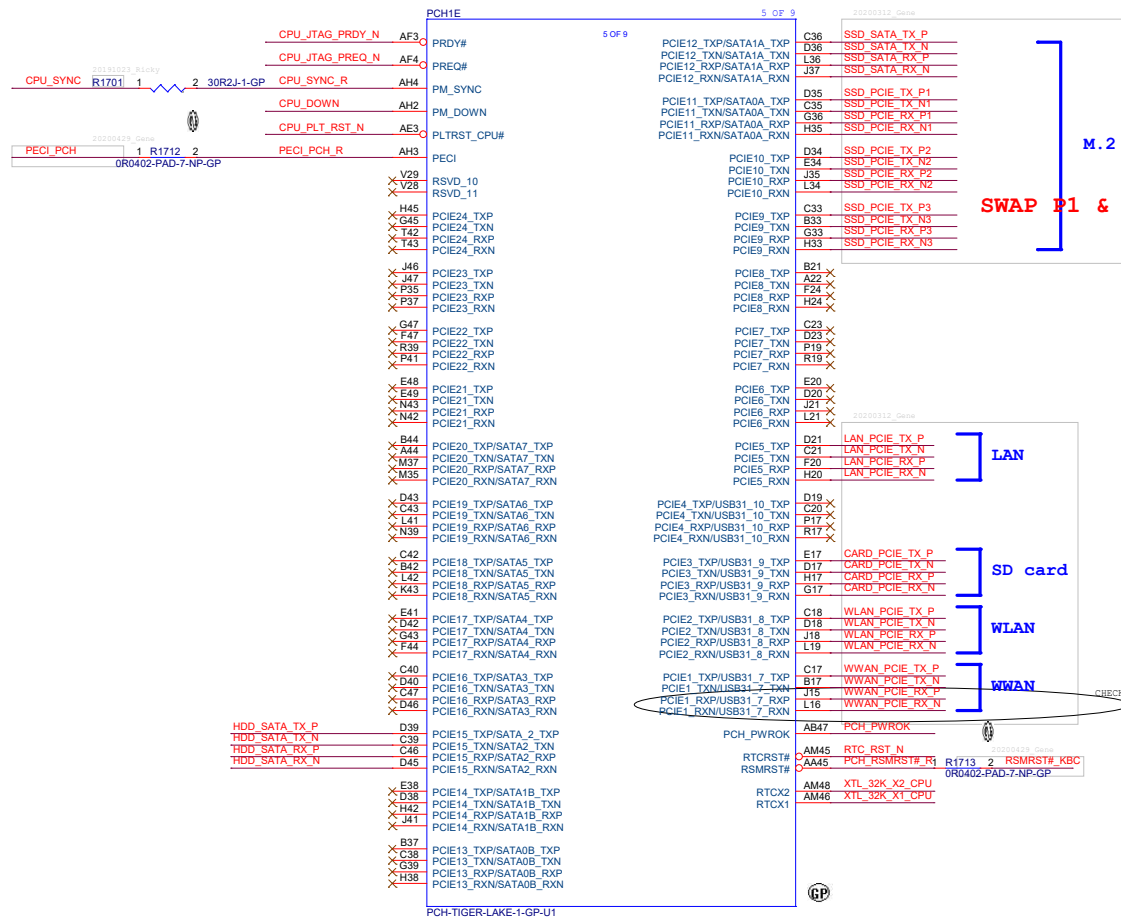
62 WWAN_PCIE_RX_N <<<-
62 WWAN_PCIE_RX_P >>>-
62 WWAN_PCIE_TX_N <<<-
62 WWAN_PCIE_TX_P >>>-

SD

33 CARD_PCIE_RX_N <<<-
33 CARD_PCIE_RX_P >>>-
33 CARD_PCIE_TX_N <<<-
33 CARD_PCIE_TX_P >>>-

HDD

60 HDD_SATA_TX_P >>>-
60 HDD_SATA_TX_N <<<-
60 HDD_SATA_RX_P <<<-
60 HDD_SATA_RX_N >>>-



Title		
017_PCH (PCIE/SATA/RTC)		
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

USB31

35 USB1_USB31_TX_P <<<=
35 USB1_USB31_TX_N <<<=
35 USB1_USB31_RX_P <<<=
35 USB1_USB31_RX_N <<<=

35 USB2_USB31_TX_P <<<=
35 USB2_USB31_TX_N <<<=
35 USB2_USB31_RX_P <<<=
35 USB2_USB31_RX_N <<<=

USB2

73 USB1_USB20_P <<<=
73 USB1_USB20_N <<<=

36 Charger_USB20_N <<<=
36 Charger_USB20_P <<<=

56 CCD_USB20_P <<<=
56 CCD_USB20_N <<<=

61 BT_USB20_P <<<=
61 BT_USB20_N <<<=

73 USB2_USB20_P <<<=
73 USB2_USB20_N <<<=

35 USB4_USB20_P <<<=
35 USB4_USB20_N <<<=

Others

6.24 THERMTRIP_CPU_N <<<=
6 PCH_2_CPU_TRIGGER >>>=
6 CPU_2_PCH_TRIGGER <<<=
68 SPI_CS_CPU_N1 <<<=
18.91.96 SPI_CS_CPU_N2 <<<=
24.53 PM_SLP_SUS_N <<<=
40 PM_SLP_LAN_N <<<=
18.68.96 SPI_SO_CPU >>>=
11.68 SPI_SI_CPU <<<=
11.68 SPI_HOLD_CPU <<<=
11.68 SPI_WP_CPU <<<=
18.68.96 SPI_CS_CPU_N0 <<<=
18.68.96 SPI_CLK_CPU <<<=
68 SYS_RESET_N >>>=
24 SYS_PWROK_R >>>=
24.62 PCH_PCIE_WAKE# <<<=
20200217V3_Willy

WWAN

62 WWAN_USB31_RX_N <<<=
62 WWAN_USB31_RX_P <<<=
62 WWAN_USB31_TX_N <<<=
62 WWAN_USB31_TX_P <<<=

WWAN

62 WWAN_USB20_N <<<=
62 WWAN_USB20_P <<<=

USH

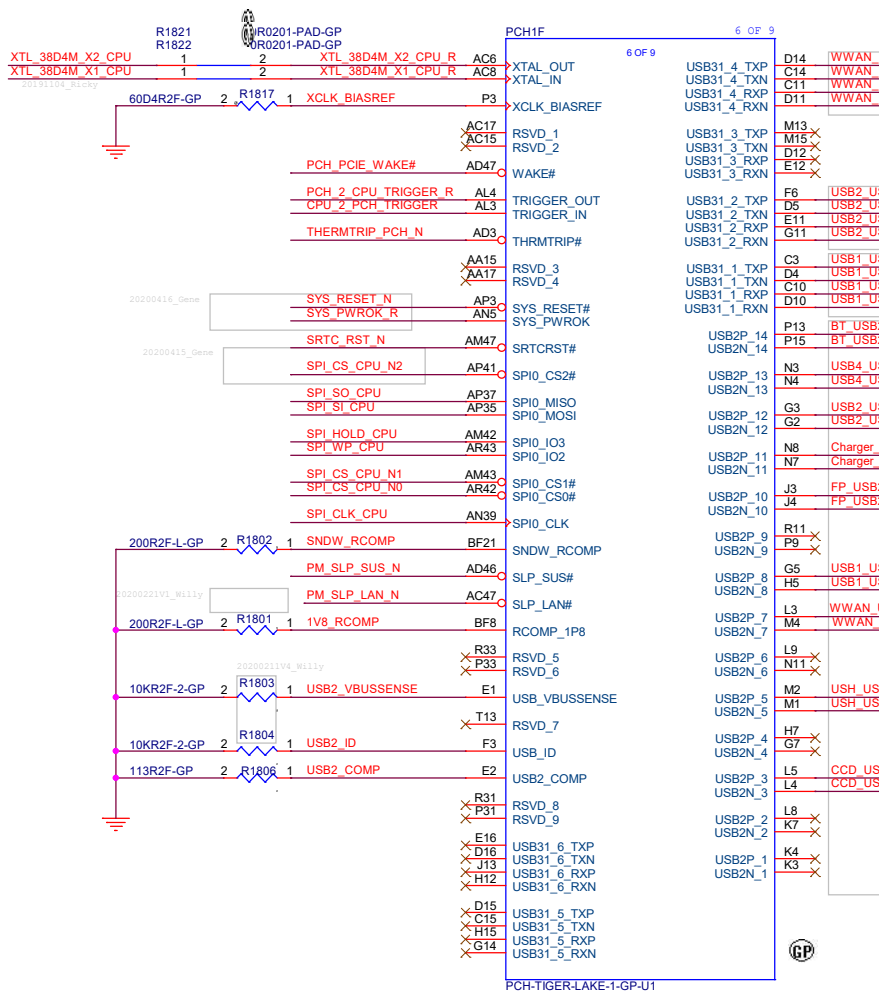
66 USH_USB20_N <<<=
66 USH_USB20_P <<<=

FPR

92 FP_USB20_P <<<=
92 FP_USB20_N <<<=

Close PCH1 (p.18)

18.68.96 SPI_CLK_CPU <<<=
18.68.96 SPI_SO_CPU <<<=
18.68.96 SPI_CS_CPU_N0 <<<=
18.91.96 SPI_CS_CPU_N2 <<<=



WWAN

20200310_Gene
D14 WWAN_USB31_TX_P
C14 WWAN_USB31_TX_N
C11 WWAN_USB31_RX_P
D11 WWAN_USB31_RX_N

USB4 Type A port2

20200310_Gene
M13 USB31_3_TXP
M15 USB31_3_TXN
D12 USB31_3_RXP
E12 USB31_3_RXN

USB3 Type A port1

20200310_Gene
F6 USB2_USB31_TX_P
D5 USB2_USB31_TX_N
E11 USB2_USB31_RX_P
G11 USB2_USB31_RX_N

BT

20200310_Gene
C3 USB1_USB31_TX_P
D4 USB1_USB31_TX_N
C10 USB1_USB31_RX_P
D10 USB1_USB31_RX_N

USB4 Type A port2

20200310_Gene
P13 BT_USB20_P
P15 BT_USB20_N

USB2 TYPEC

20200310_Gene
N3 USB4_USB20_P
N4 USB4_USB20_N

USB3 Type A port1

20200310_Gene
G3 USB2_USB20_P
G2 USB2_USB20_N

FP

20200310_Gene
N8 Charger_USB20_P
N7 Charger_USB20_N

USB1 TYPEC

20200310_Gene
J3 FP_USB20_P
J4 FP_USB20_N

WWAN

20200310_Gene
R11 P9
G5 USB1_USB20_P
H5 USB1_USB20_N

USH

20200310_Gene
L3 WWAN_USB20_P
M4 WWAN_USB20_N

Camera

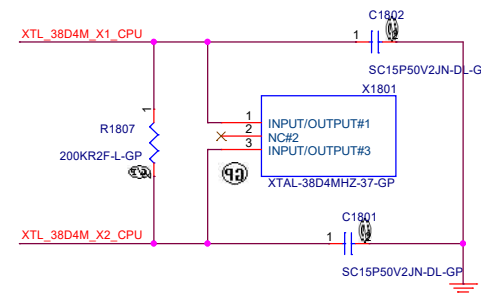
20200310_Gene
L9 N11
M2 USH_USB20_P
M1 USH_USB20_N

SYS_PWROK_R R1816 1 2 100KR2J-1-GP

PM_SLP_SUS_N R1818 1 2 100KR2J-1-GP

PM_SLP_LAN_N R1819 1 2 100KR2J-1-GP

SPI_CLK_CPU R1820 1 2 100KR2J-1-GP



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

Title 018_PCH (USB31/USB2/SPI/XTAL)

Size A3 Document Number Broadmoor 15 TGL-H Rev A00

Date: Friday, March 12, 2021 Sheet 18 of 106

63 SSD2_CLK_CPU_P <<<—
63 SSD2_CLK_CPU_N <<<—

63 SSD_CLK_CPU_P >>>—
63 SSD_CLK_CPU_N >>>—

```
76 GFX_CLK_CPU_P    >>>=
76 GFX_CLK_CPU_N    >>>=
```

```

97 LAN_CLK_CPU_P    >>>=
97 LAN_CLK_CPU_N    >>>=

```

```

61 WLAN_CLK_CPU_P  >>> ---
61 WLAN_CLK_CPU_N  >>> ---

```

61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_CLKP
61 CNV_WT_CLKN

```

61 CNV_WR_DP1      ~~~~~~
61 CNV_WR_DN1      ~~~~~~
61 CNV_WR_DP0      ~~~~~~
61 CNV_WR_DN0      ~~~~~~
61 CNV_WR_CLKP     ~~~~~~
61 CNV_WR_CLKN     ~~~~~~

```

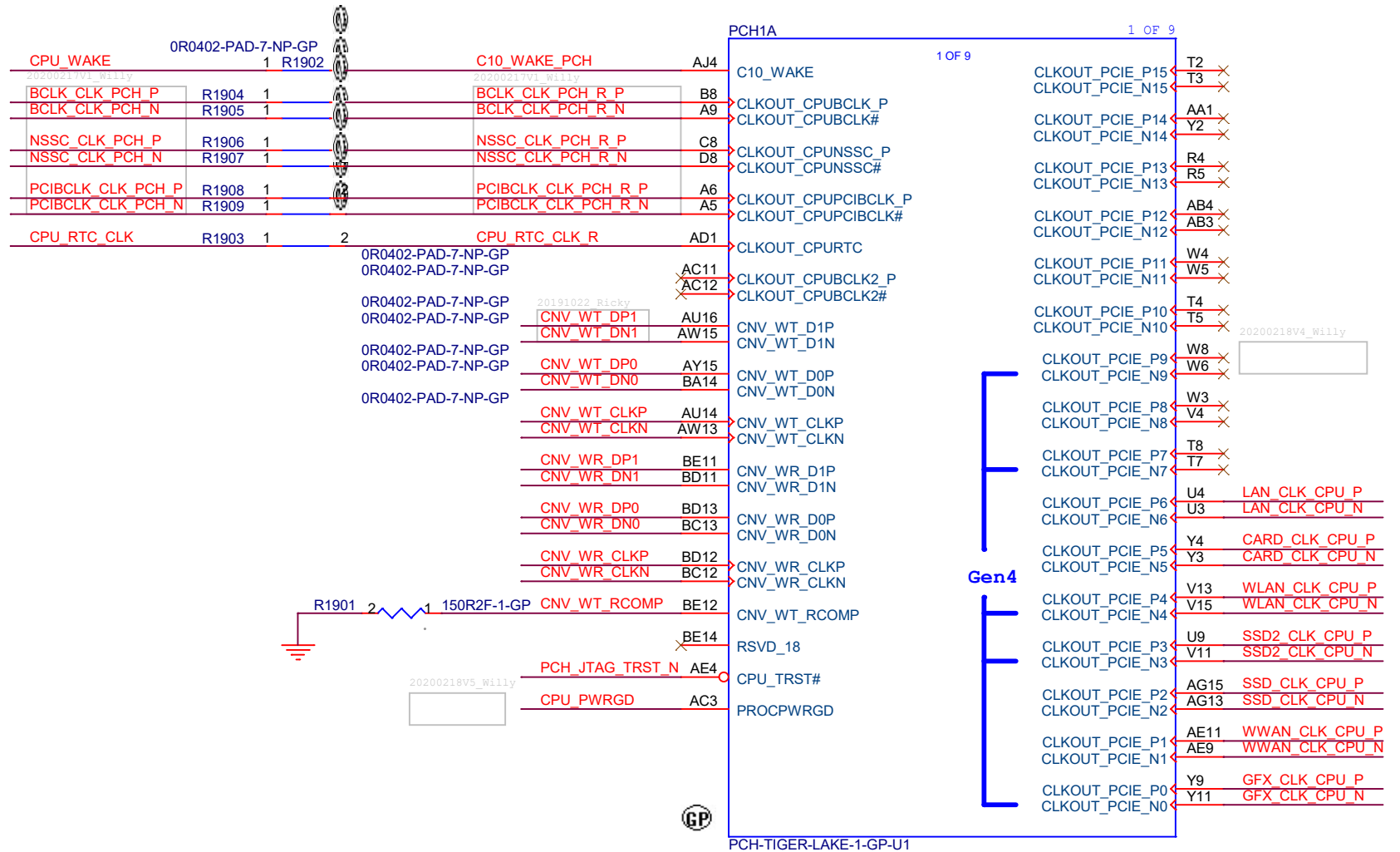
```
62  WWAN_CLK_CPU_P <<<—
62  WWAN_CLK_CPU_N <<<—
```

33 CARD_CLK_CPU_N <<<—
33 CARD_CLK_CPU_P <<<—

```

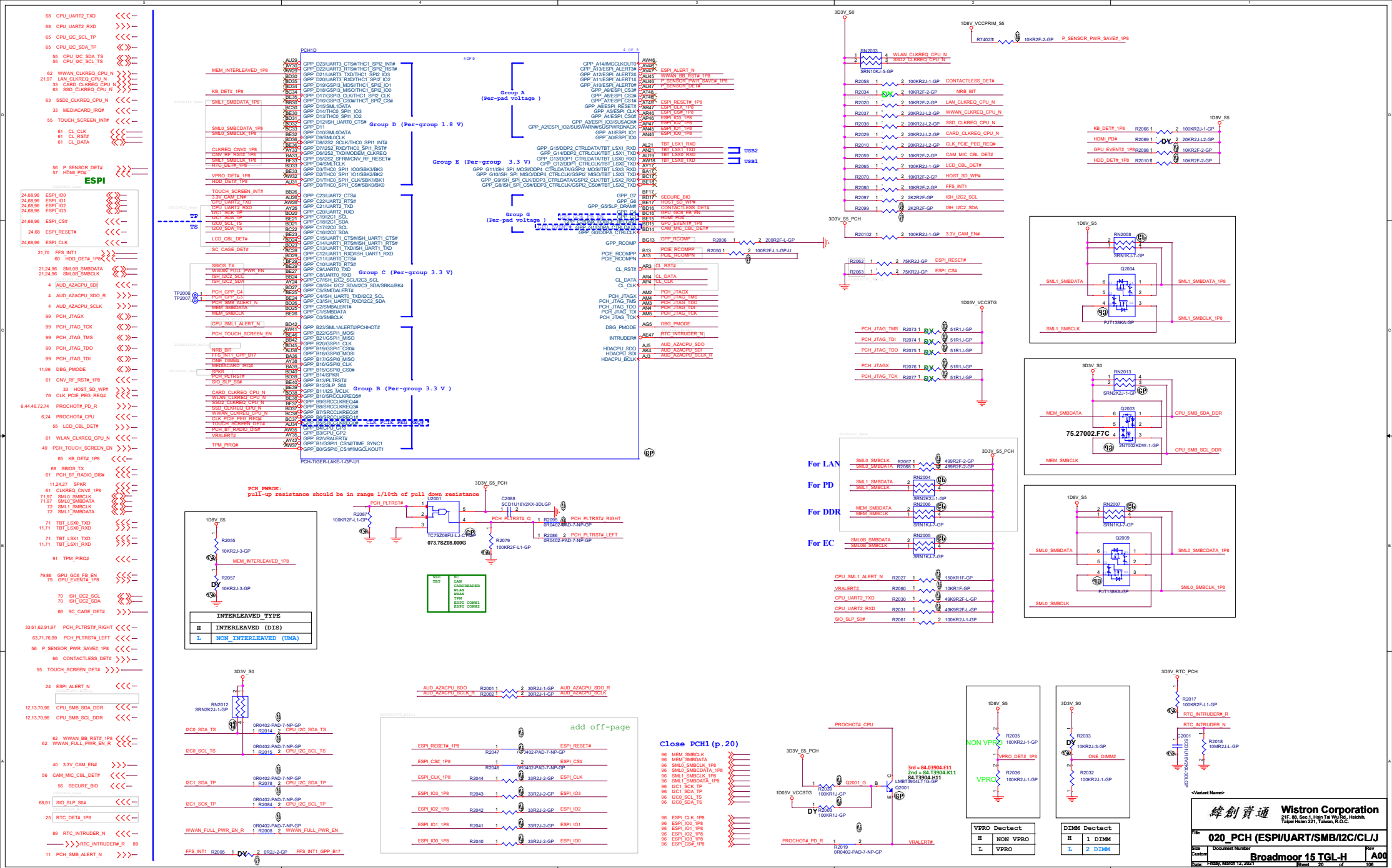
6 CPU_WAKE >>>-
99 PCH_JTAG_TRST_N <<<-
20191023 Ricky
6 CPU_PWRGD <<<-
20200217V1 W11ly
6 BCLK_CLK_PCH_P <<<-
6 BCLK_CLK_PCH_N <<<-
6 NSSC_CLK_PCH_P <<<-
6 NSSC_CLK_PCH_N <<<-
6 PCIBCLK_CLK_PCH_P <<<-
6 PCIBCLK_CLK_PCH_N <<<-
6 CPU_RTC_CLK <<<-

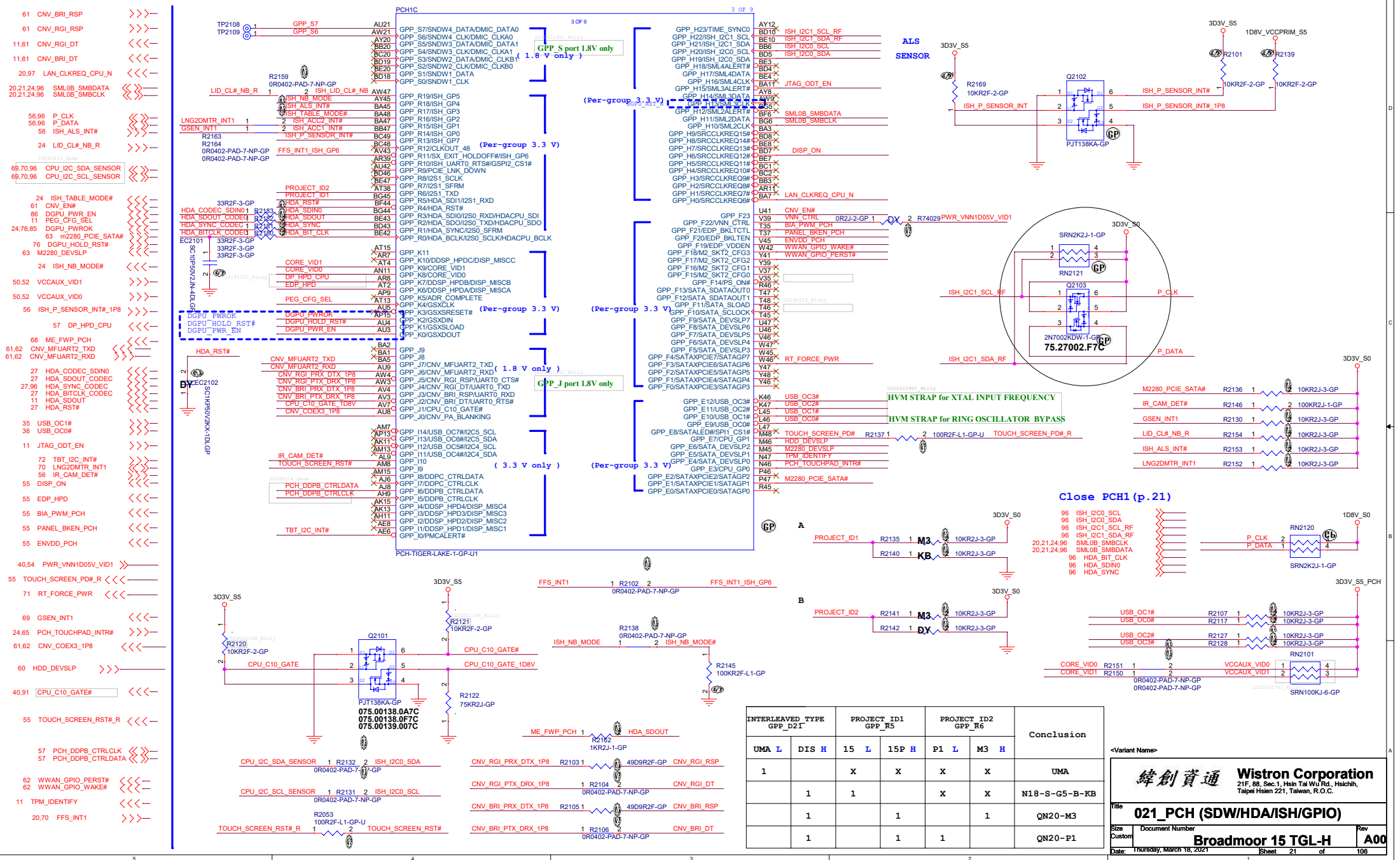
```



CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	0	Yes	PCI Express* Clock Output: PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices. <ul style="list-style-type: none"> CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support
--	---	-----	--

 <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div>	
Title	
019_PCH (CLK/CNVi)	
Size A4	Document Number <div>Broadmoor 15 TGL-H</div>
Date:	Rev
Friday, March 12, 2021	A00
Sheet	106
19	of





INTERLEAVED TYPE		PROJECT ID1		PROJECT ID2		Conclusion
GFP_D2T	GFP_R5	GFP_R6				
UMA L	DIS H	15 L	15P H	P1 L	M3 H	
1		X	X	X	X	UMA
1	1			X	X	N18-S-G-B-KB
1		1			1	QN20-M3
1		1		1		QN20-P1

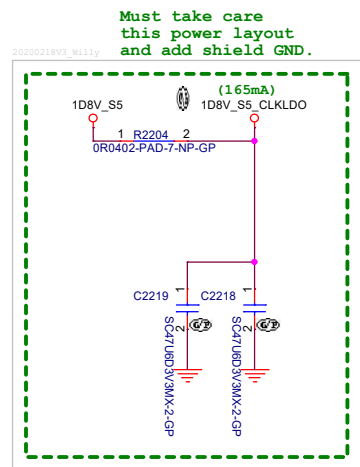
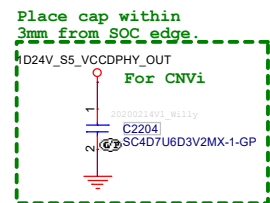
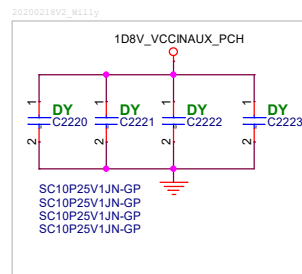
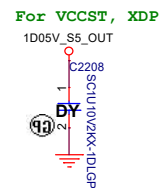
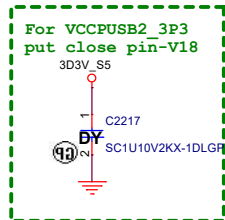
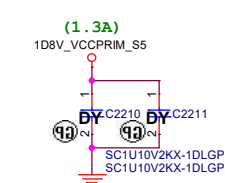
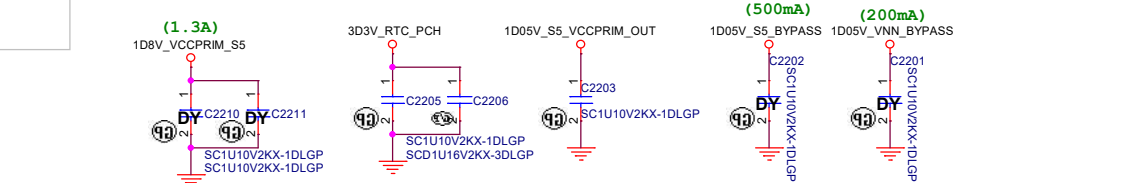
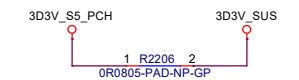
~Variant Name~

緯創資通

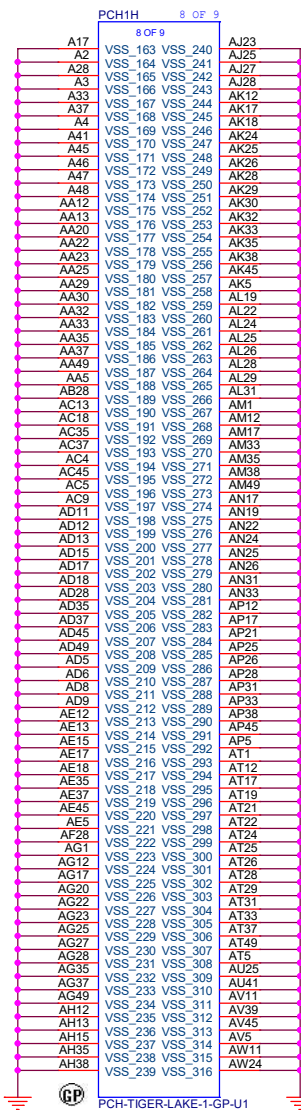
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

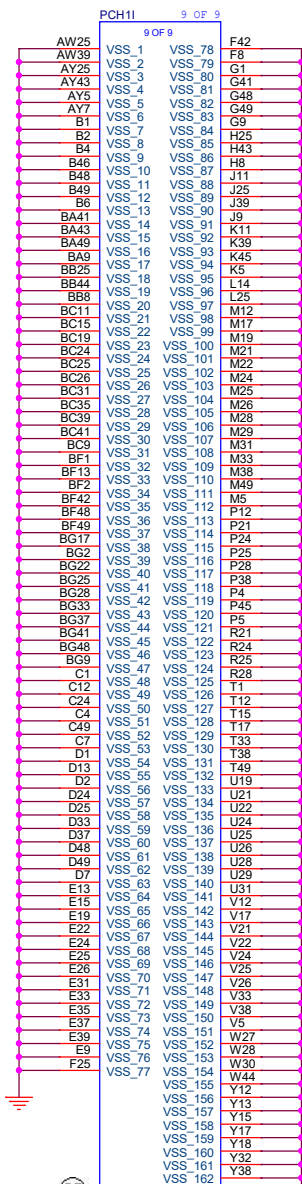
Title			021_PCH (SDW/HDA/ISH/GPIO)		
Size	Document Number	Broadmoor 15 TGL-H		Rev	A00
Date	Thursday, March 18, 2021	Sheet	21	of	106



Power Rail	Decap Placement	Form Factor	Value	Number
VCCA_CLKLDO_IP 8	Primary Side	0603	47uF	1



PCH-TIGER-LAKE-1-GP-U1



PCH-TIGER-LAKE-1-GP-U1

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 023_PCH (VSS)

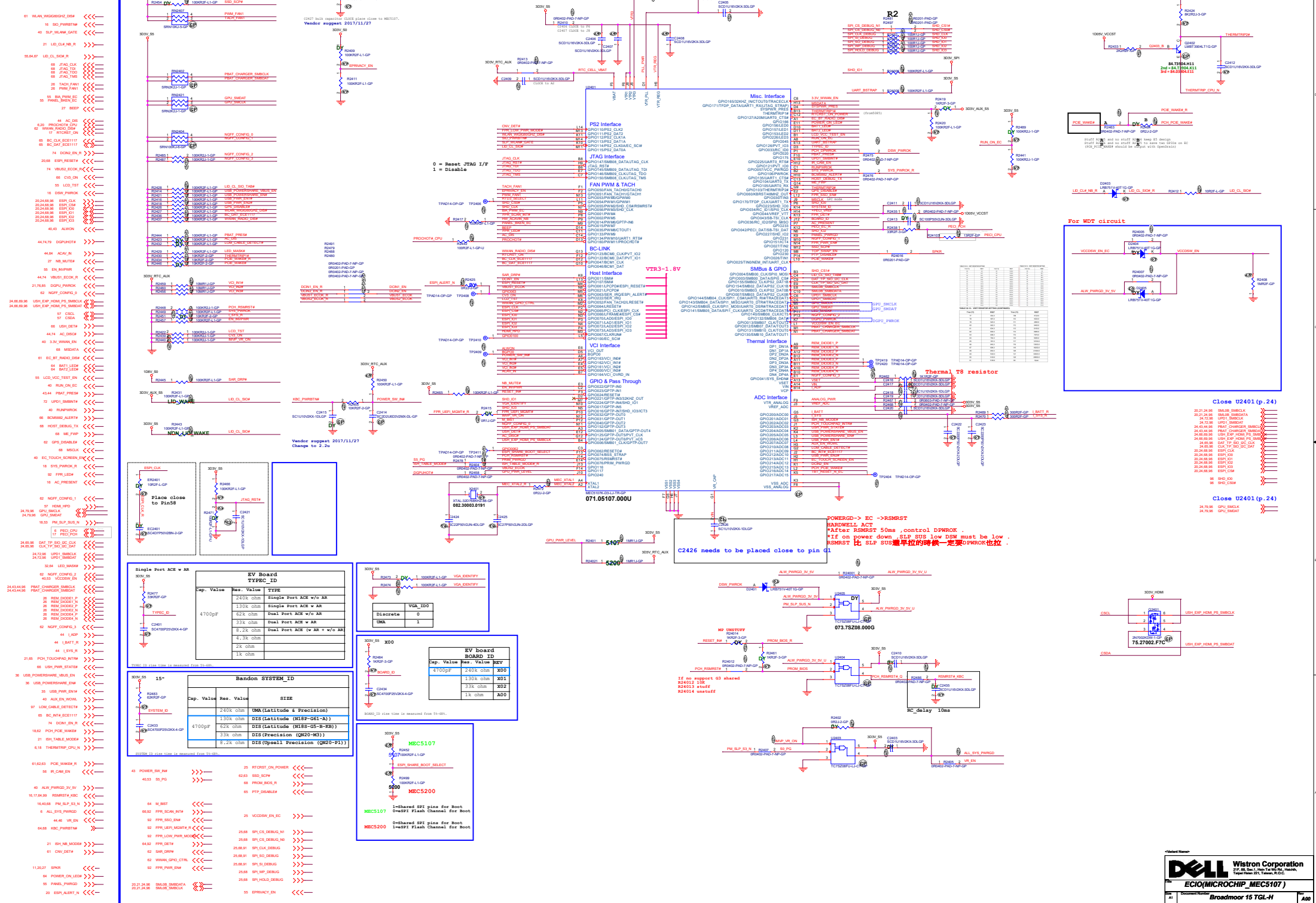
Size A3 Document Number

Broadmoor 15 TGL-H A00

Date: Friday, March 12, 2021

Sheet 23 of 106

Main Func = EC



SYSTEM SPI ROM

24,68,91	SPI_CLK_DEBUG	>>>>	_____
24,68,91	SPI_SI_DEBUG	>>>>	_____
24,68,91	SPI_SO_DEBUG	>>>>	_____
24,68	SPI_WP_DEBUG	>>>>	_____
24,68	SPI_HOLD_DEBUG	>>>>	_____
24,68	SPI_CS_DEBUG_N0	>>>>	_____
24,68	SPI_CS_DEBUG_N1	>>>>	_____

```

24 VCCDSW_EN_EC >>>_____
24 RTCRST_ON_POWER >>>_____
20 RTC_DET#_1P8 <<<_____

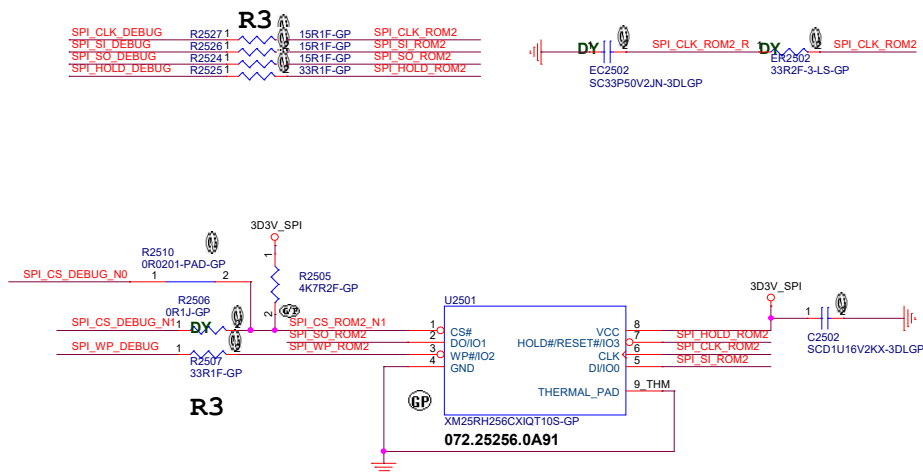
```

Close U2501 (p.25)

```

96  SPI_CLK_ROM2
96  SPI_SI_ROM2
96  SPI_CS_ROM2 N1

```



Non-vPRO configs - 16MB (UI)
Winbond W25Q128JVSQ; MXIC: MX25L12873FM; GigaDevice:
GD25B127D
If more than 3 sources are required then these parts can be
considered:
Spansion: S25FL128L; Micron: MT25QL128ABA1E0-OSIT

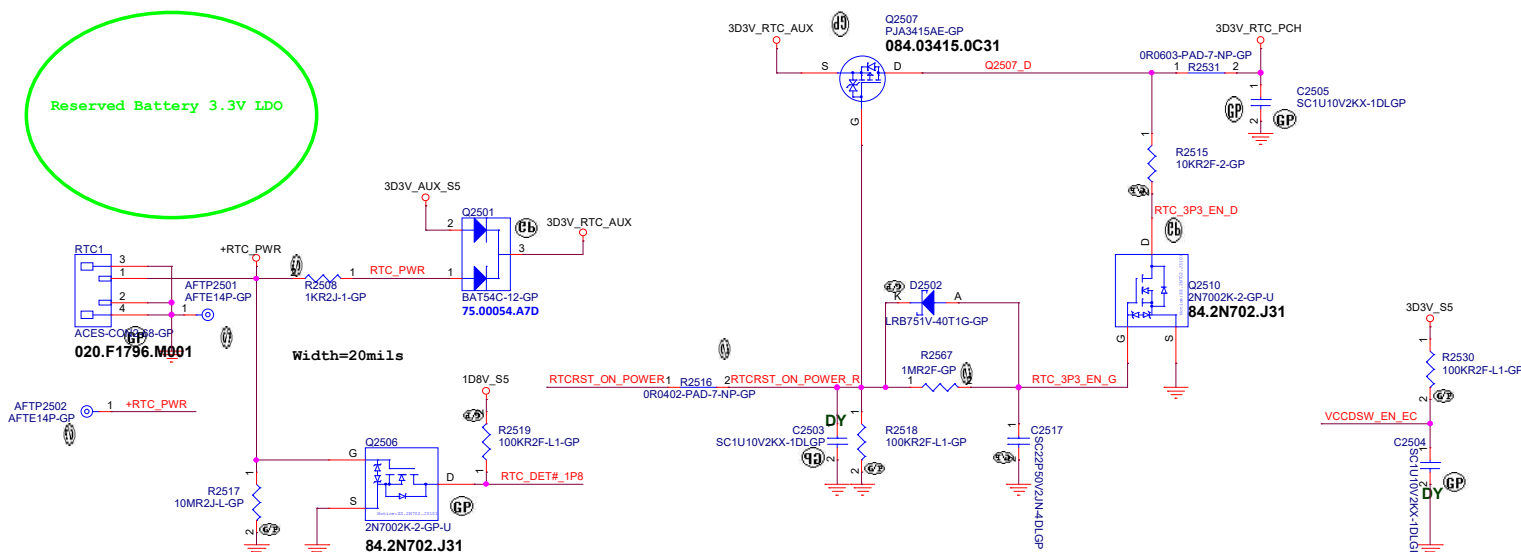
vPRO Configs: 32MB
Winbond W25Q256JV, Gigadevice GD25Q256C, Cypress
S25FL256L

Winbond		W53CN (8uB)		8-pin S0CK 28-mil	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.25064.0E03	W25Q64VEIQ	072.25064.0F01	W25Q64VFSIQ
16M Byte	128M bit	072.25128.0A11	W25Q128VEIQ	072.25128.0B51	W25Q128VFSIQ
32M Byte	256M bit	072.25256.0N01	W25Q256VEIQ		N/A

MXIC		W53CN (8uB)		8-pin S0CP (20mil)	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.25643.0J01	MX25L643F2E1	072.25647.0000	MX25L643F2E1-08G
16M Byte	128M bit	XX	XX	72.12833.001	MX25L1283F2E1-10J
32M Byte	256M bit	072.25673.0003	MX25L25673F2E1-08G	072.25673.0001	MX25L25673CM21-08G

GG46VE7CE		W53CN (8uB)		S0FP 208MIL	
ROM size		Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
8M Byte	64M bit	072.25643.0J01	GD25B64C1GR	072.25664.0C01	GD25B64C1GR
16M Byte	128M bit			072.25127.0001	GD25B127D81GR
32M Byte	256M bit	072.25656.0F03	GD25B256C1GR		

X09 design DS3 Non-DS3 with RTC power gating



<Variant Name>

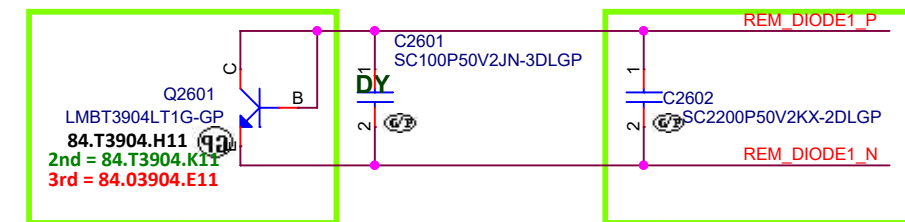
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				Flash/RTC			
Size	Document Number						Rev
Custom	Broadmoor 15 TGL-H						A00
Date: Friday, March 12, 2021				Sheet 25 of		106	

Main Func = Thermal / FAN

24 REM_DIODE1_P
24 REM_DIODE1_N
24 REM_DIODE2_P
24 REM_DIODE2_N

24 REM_DIODE4_P
24 REM_DIODE4_N
24 PWM_FAN1
24 TACH_FAN1

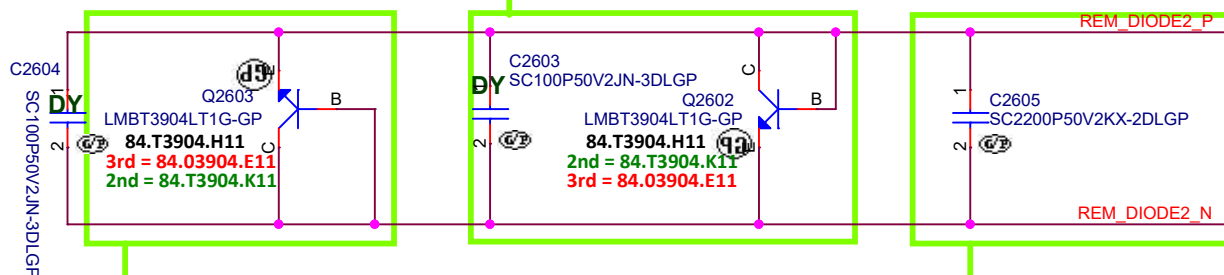


Layout Note: Place to CPU

Layout Note: Close to EC

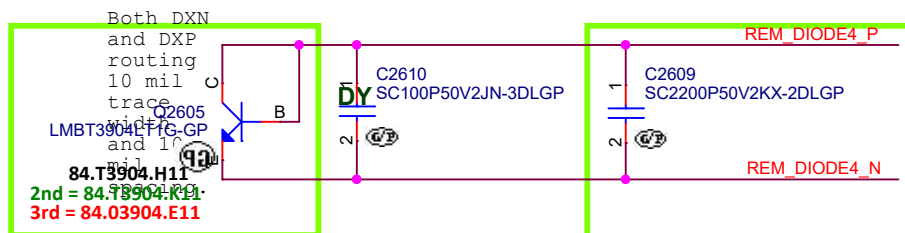
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to WWAN/ SSD2



Layout Note: Close to SSD1

Layout Note: Close to EC

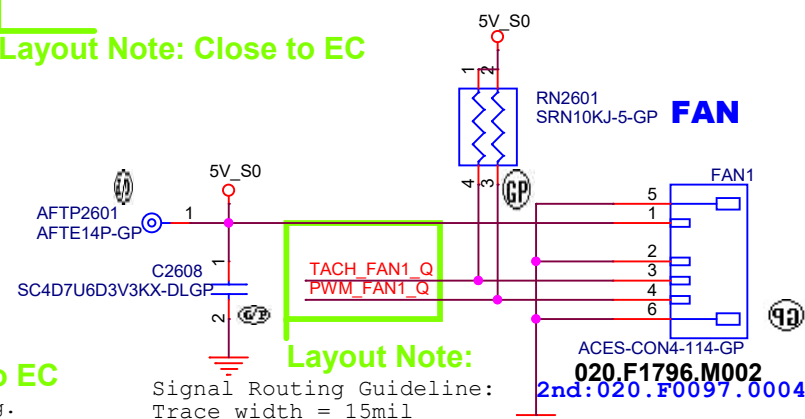
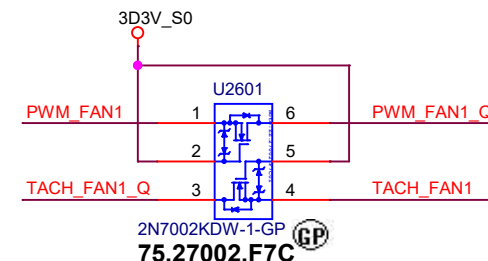


Layout Note: Place to DIMM

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

5107/5200 Channel	Location	Function
DP1/DN1	(Q2601)	For OTP, T8 shut down
DN2A/DP2A	(Q2602)	For ambient temp.
DN2A/DP2A	(Q2603)	For SSD temp
DP4/DN4	(Q2605)	For skin hot spot



Signal Routing Guideline:
Trace width = 15mil

<Variant Name>



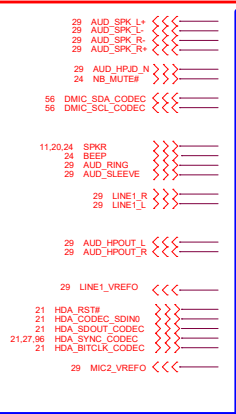
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **INT IO (Thermal/Fan)**

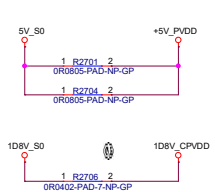
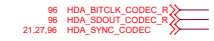
Size A4 Document Number **Broadmoor 15 TGL-H** Rev **A00**

Date: Friday, March 12, 2021 Sheet 26 of 106

Main Func = Audio



Close U2701 (p.27)



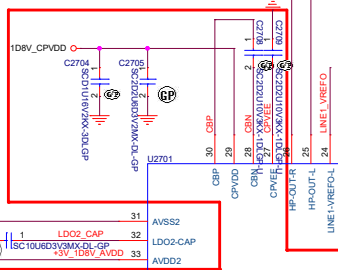
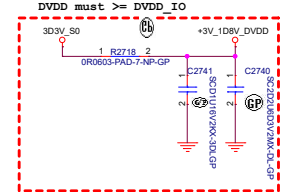
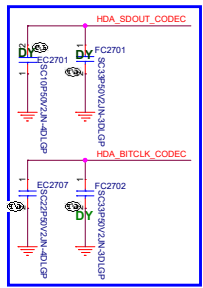
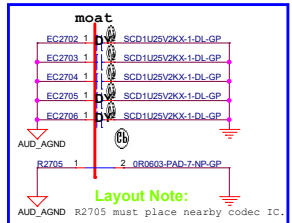
Audio Codec Chip ALC3204

Analog
Digital

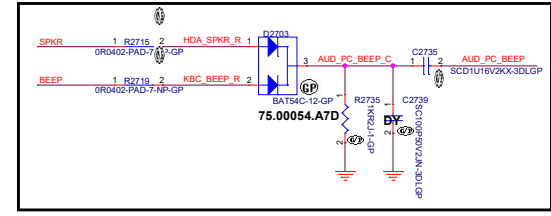
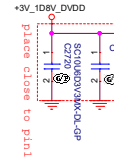
1.8V power rail should be supplied by linear regulator, not switching regulator. If switch regulator is available, please make sure that switch frequency operates at out-of-band (over 200KHz)

>2A moat

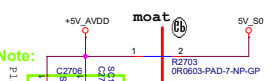
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



ALC3204
QFN40 (5X5)
071.03204.M001



Layout Note:

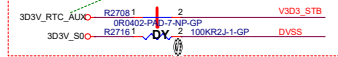


Place close to Pin 20

Analog
Digital
moat

Open drain output, pull up to DVDD or max. 5V

For RTC Gen9 reset circuit change power rail.




Close to U2701 pin12

<Variant Name>

5	4	3	2	1
D				
C				
B				
A				

<Variant Name>

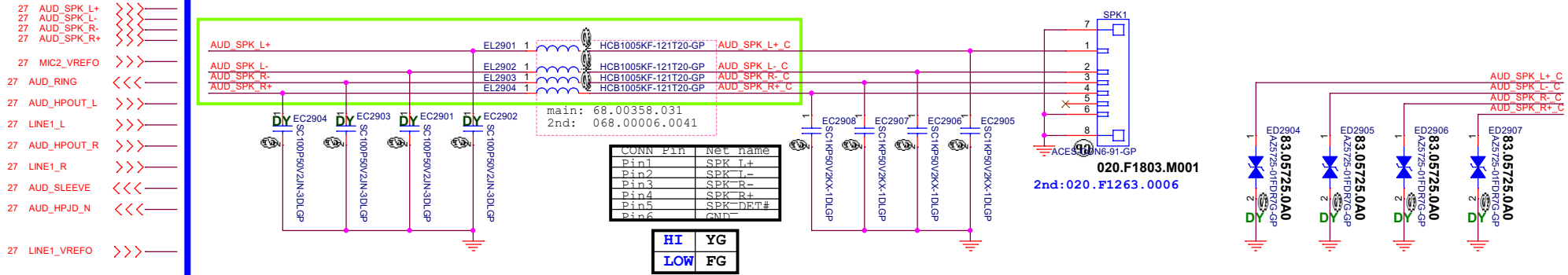
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (RSVD) (Audio AMP)			
Size A4	Document Number Broadmoor 15 TGL-H		Rev A00
Date: Friday, March 12, 2021		Sheet 28 of	106

Main Func = Audio

Layout Note:

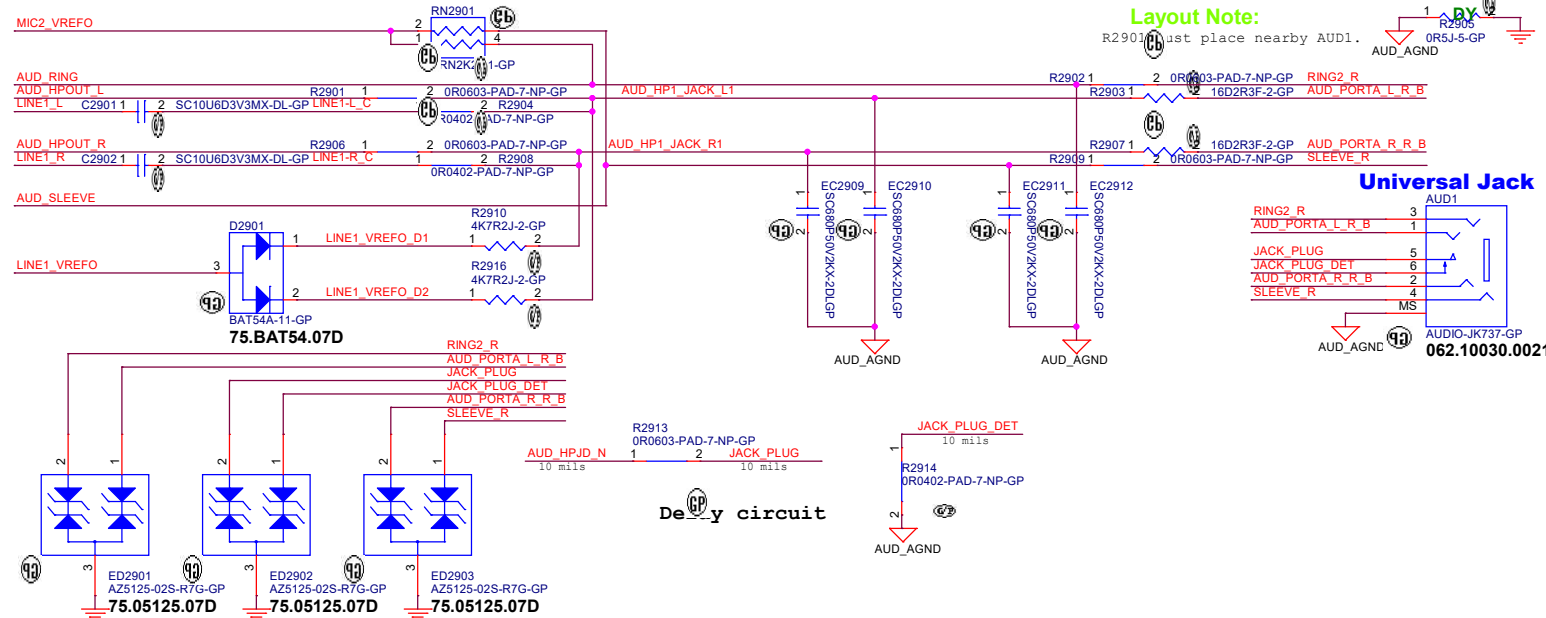
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

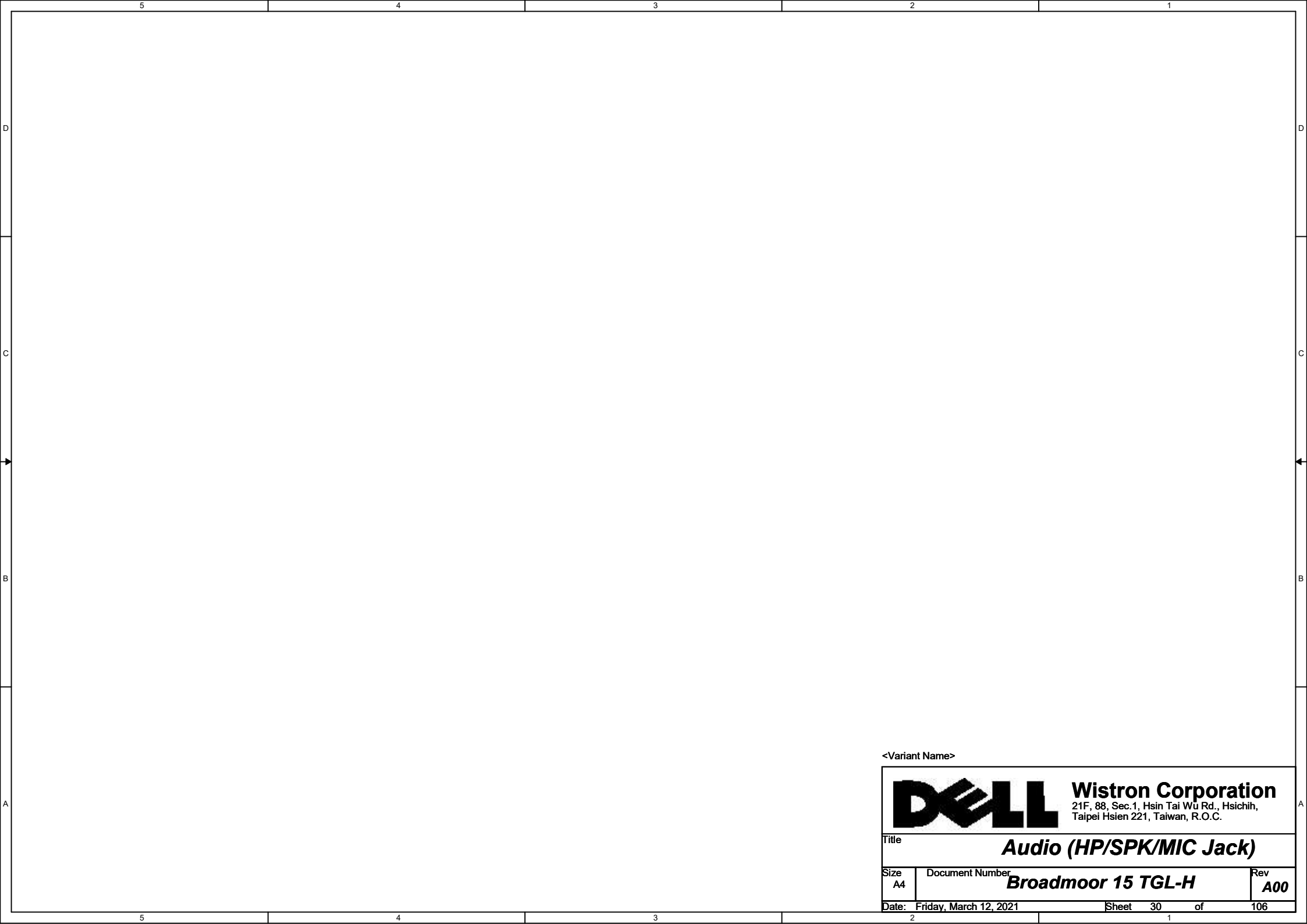


Layout Note:


R2901 must place nearby AUD1.



<Variant Name>




<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (HP/SPK/MIC Jack)			
Size A4	Document Number Broadmoor 15 TGL-H		Rev A00
Date: Friday, March 12, 2021		Sheet 30 of	106

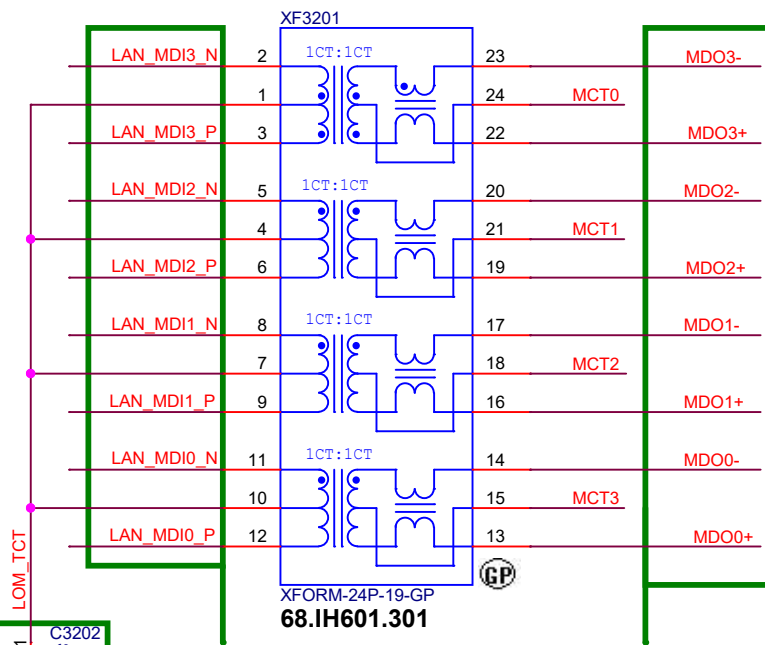
5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN (RSVD)			
Size A4	Document Number Broadmoor 15 TGL-H		Rev A00
Date: Friday, March 12, 2021		Sheet 31 of	106

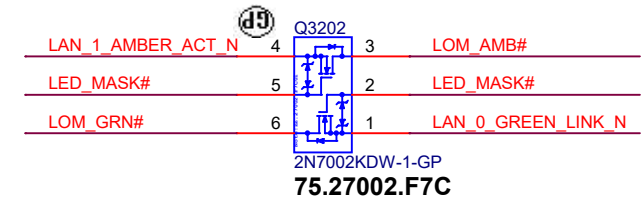
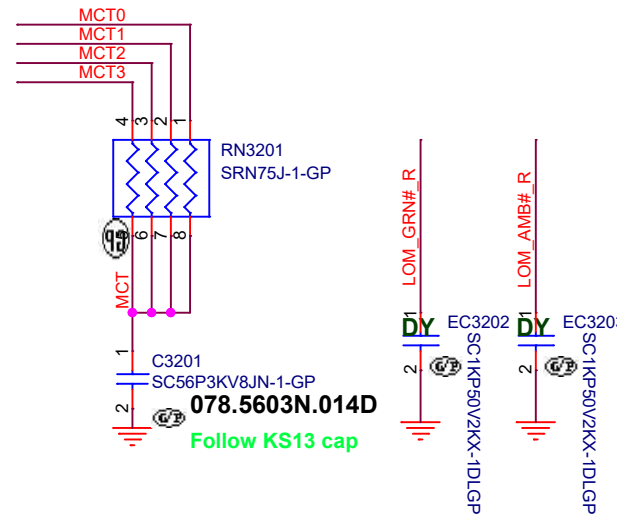
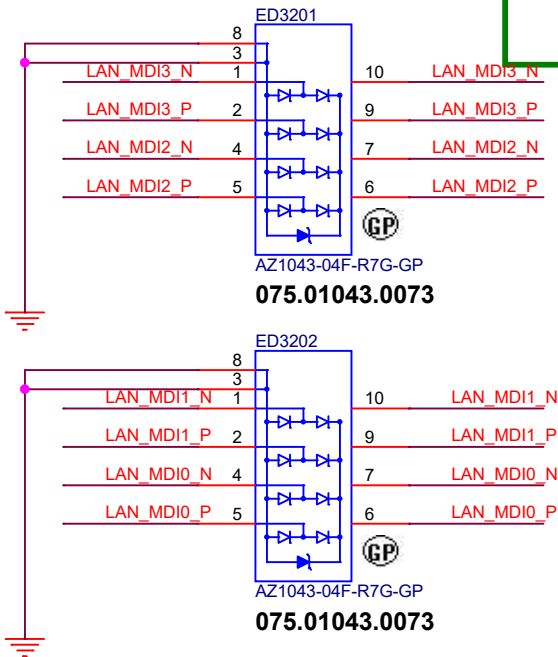
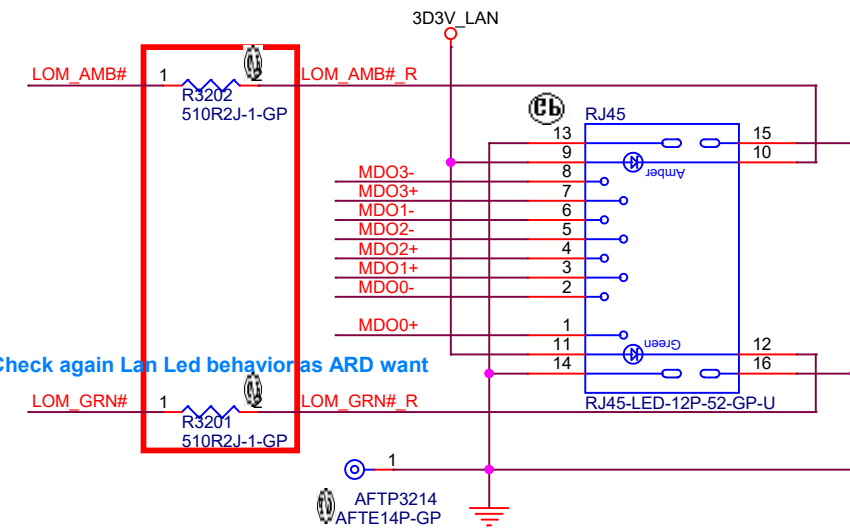
Main Func = LAN

24,64 LED_MASK#
97 LAN_0_GREEN_LINK_N
97 LAN_1_AMBER_ACT_N
97 LAN_MDI0_P
97 LAN_MDI0_N
97 LAN_MDI1_P
97 LAN_MDI1_N
97 LAN_MDI2_P
97 LAN_MDI2_N
97 LAN_MDI3_P
97 LAN_MDI3_N



Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

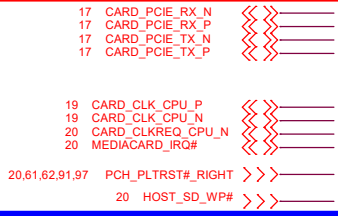
<Variant Name>

DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title LAN (RSVD) (RJ45+Transformer)		
Size A4	Document Number Broadmoor 15 TGL-H	Rev A00
Date: Friday, March 12, 2021		Sheet 32 of 106

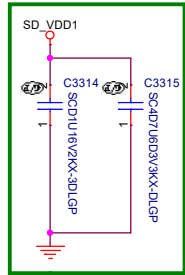
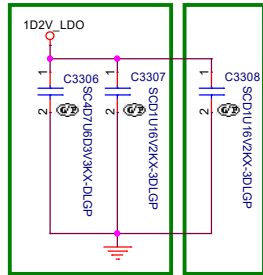
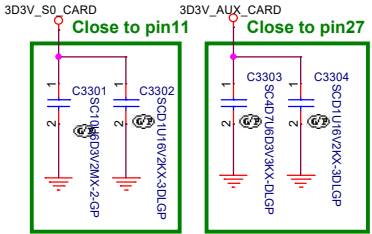
Main Func = Card Reader

3D3V_S0_CARD

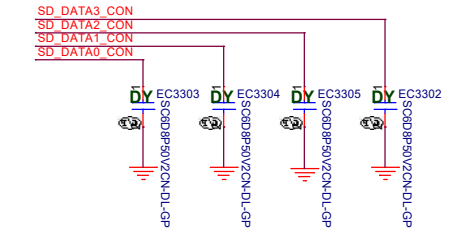
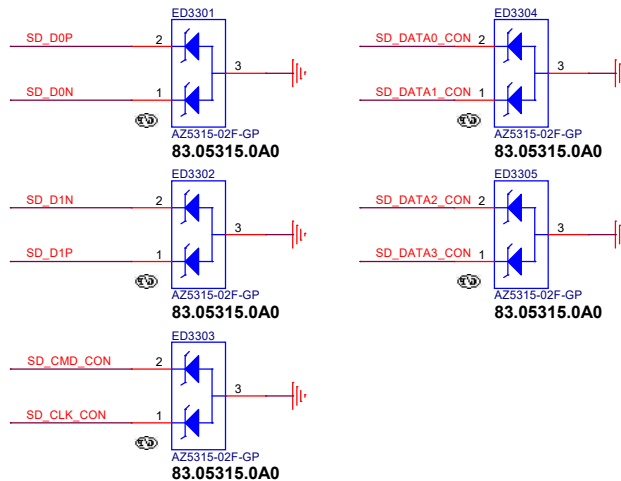
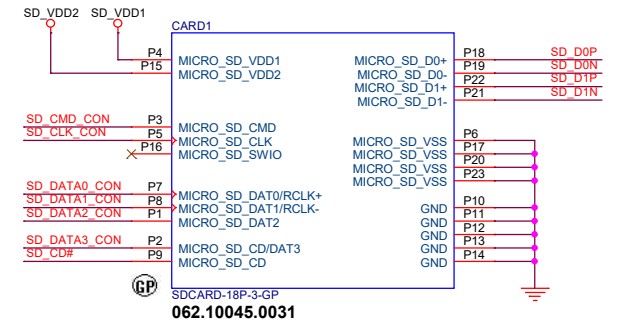
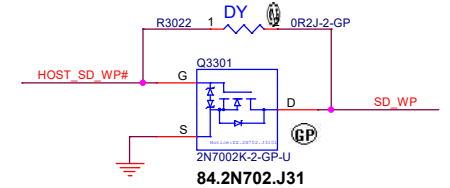
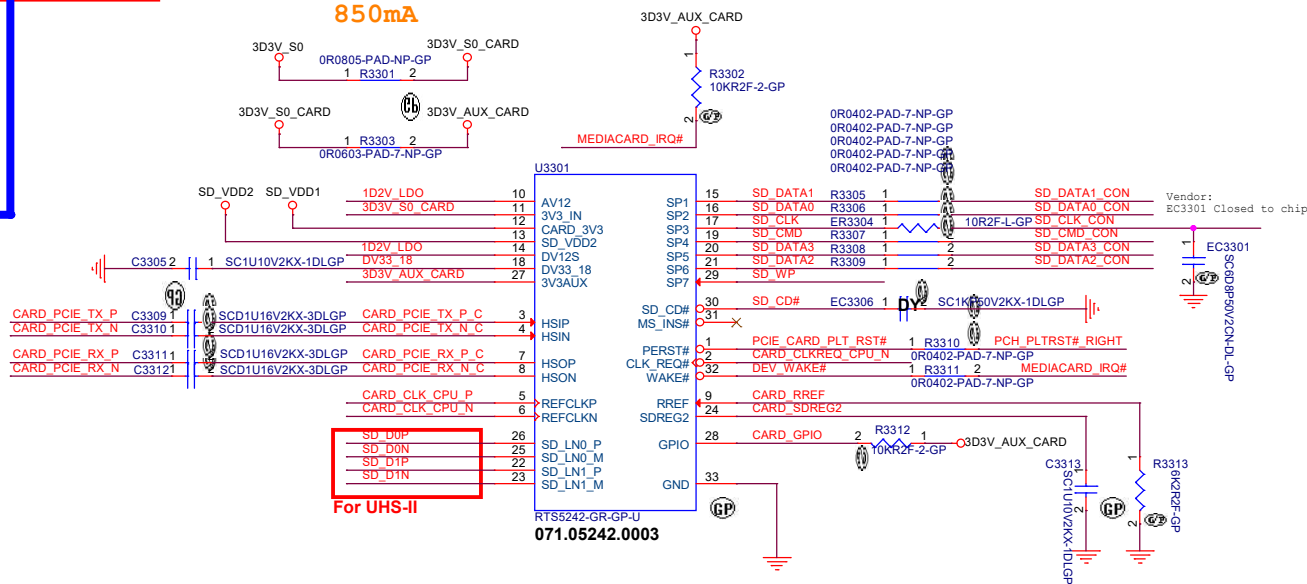
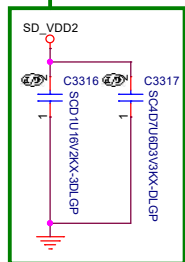
850mA

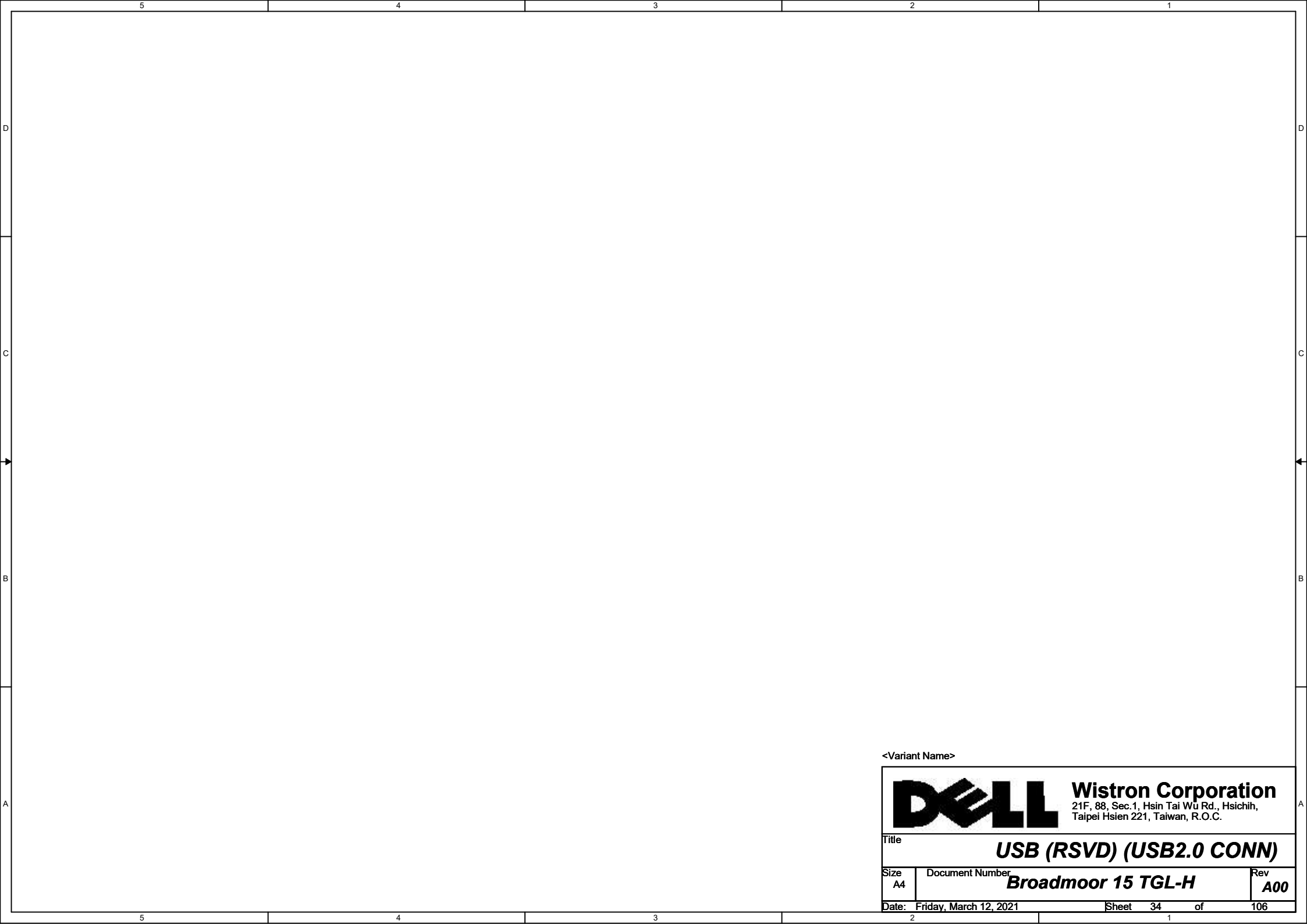


Layout Note:




Layout Note:Close to Card Reader CONN



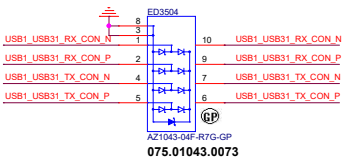
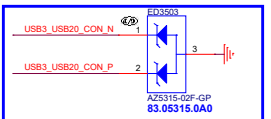
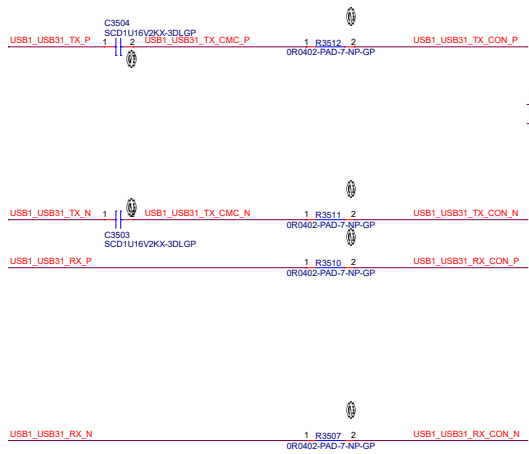
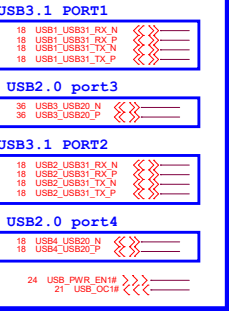


<Variant Name>

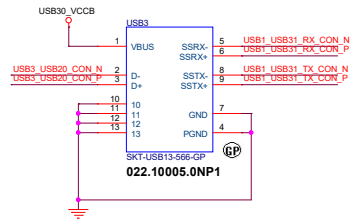
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title USB (RSVD) (USB2.0 CONN)					
Size A4	Document Number Broadmoor 15 TGL-H				Rev A00
Date: Friday, March 12, 2021			Sheet 34 of 106		

Main Func = USB 3.0

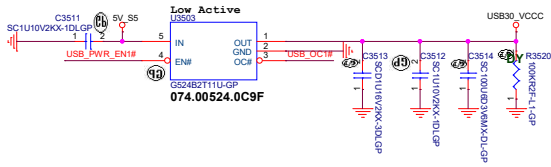
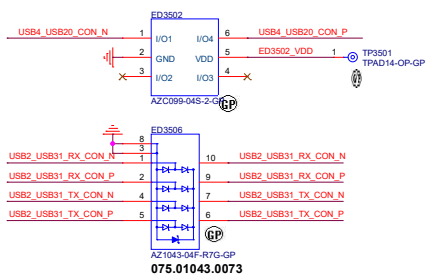
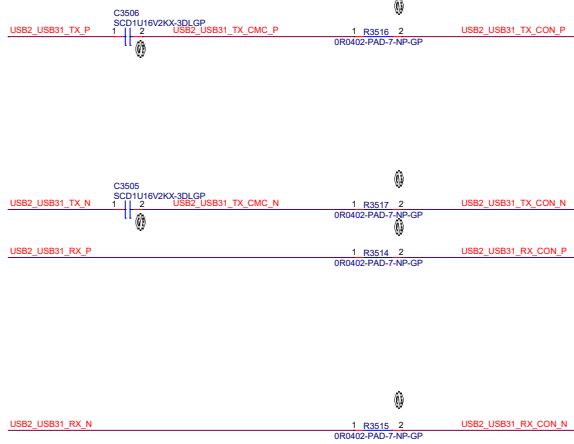
USB3/USB32-1/USB20-3/PowerShare



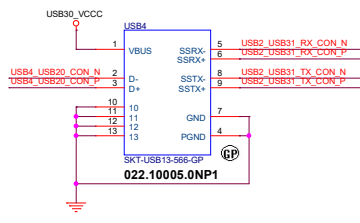
EXT Port1 Right Side, Support Power Share



USB4/USB32-2/USB20-4



EXT Port1 Right Side, Support Power Share

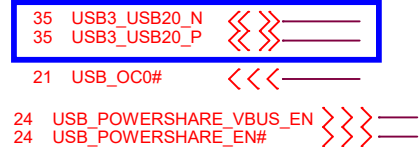


<Variant Name>

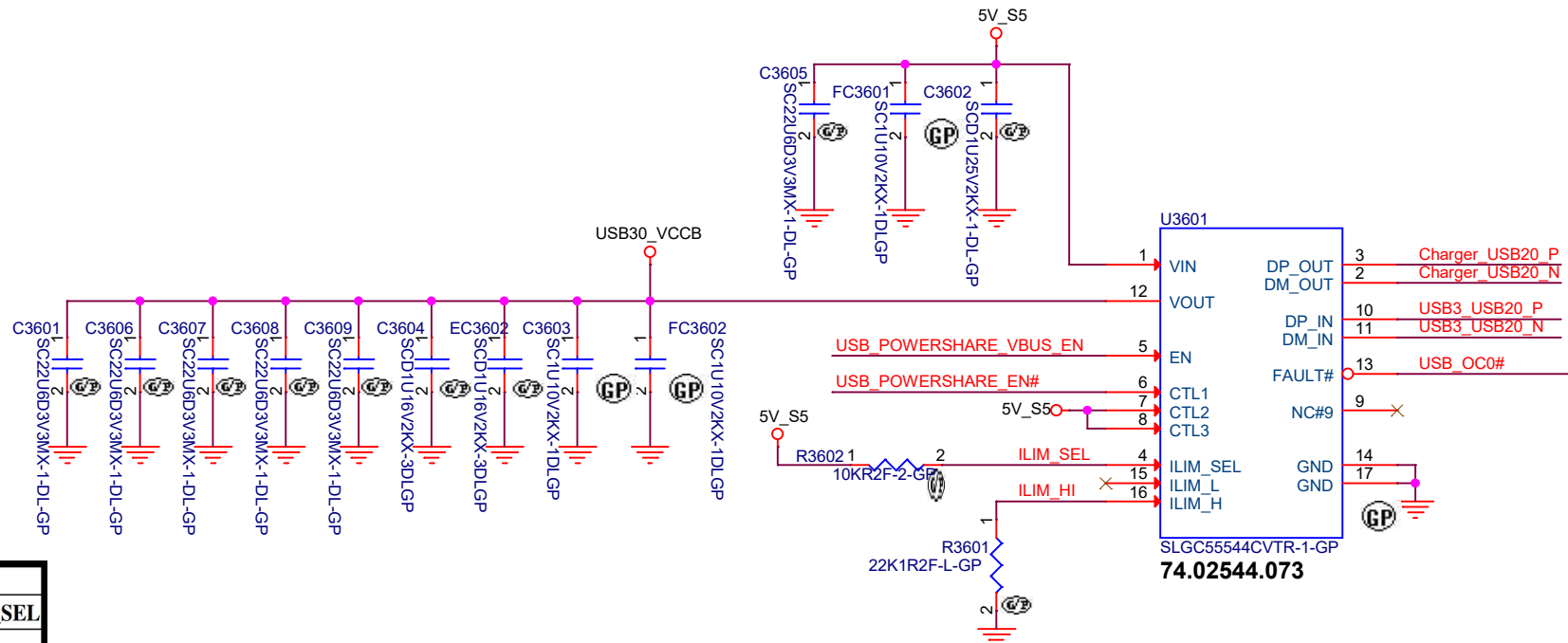
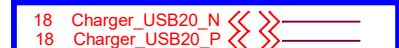
Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

USB2.0 port3



USB charger



Device Control Pins

Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

<Variant Name>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (USB Charger)

Size
A4

Document Number

Broadmoor 15 TGL-H


Rev
A00

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5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title USB (RSVD) (PCIE to USB3.0)					
Size A4	Document Number Broadmoor 15 TGL-H				Rev A00
Date: Friday, March 12, 2021			Sheet 37 of 106		


5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title USB (RSVD) (USB Redriver/Hub)					
Size A4		Document Number Broadmoor 15 TGL-H			Rev A00
Date: Friday, March 12, 2021			Sheet 38 of 106		

5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sequence (RSVD)			
Size A4	Document Number Broadmoor 15 TGL-H		Rev A00
Date: Friday, March 12, 2021		Sheet 39 of	106

Main Func = Power Plane EN Sequence

2443 ALWON >>>
45 3V3V_EN <<<
45 3V3V_PG <<<
45 3V3V_PG <<<
24 ALW_PWDN <<<
18 PM_SLP_LAN_N >>>
24 SLP_WLAN_GATE >>>
18 SLP_SLP_WLAN >>>
24 ALW_EN_WWAN >>>
24 3V3V_WWAN_EN >>>

2191 CPU_CIS_GATE >>>
27 RUN_ON_R >>>
2435 VCCSTG_EN >>>

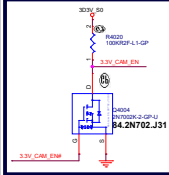
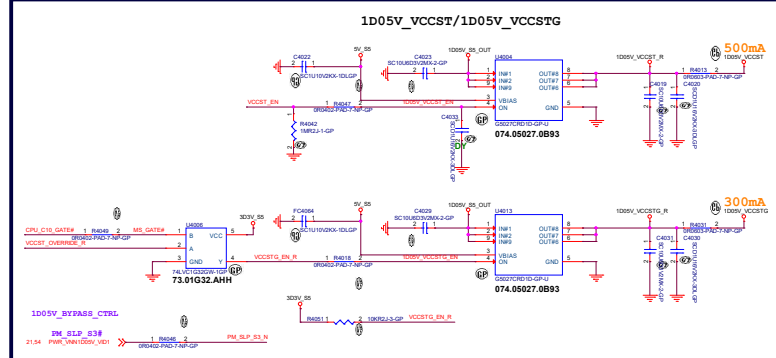
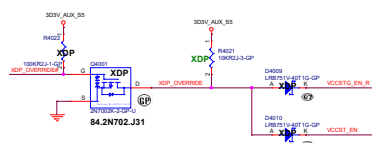
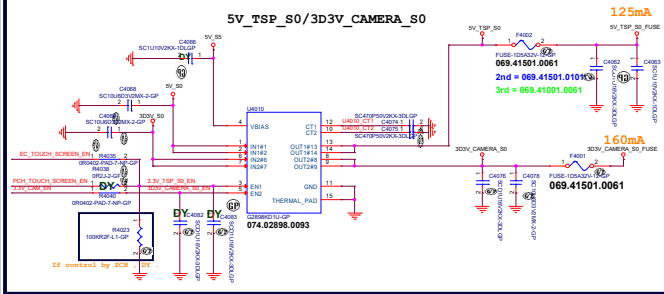
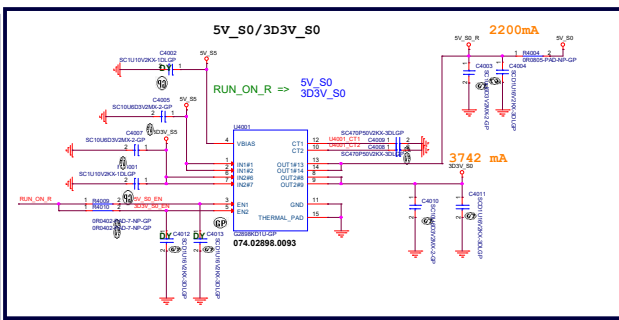
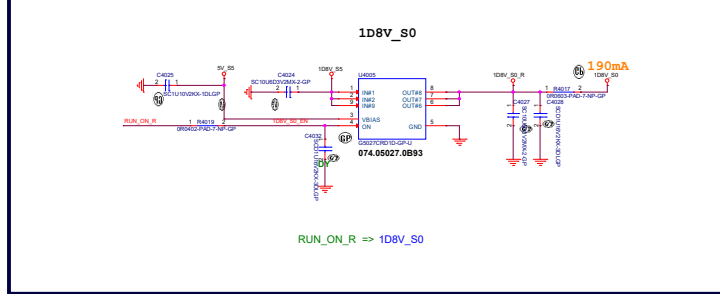
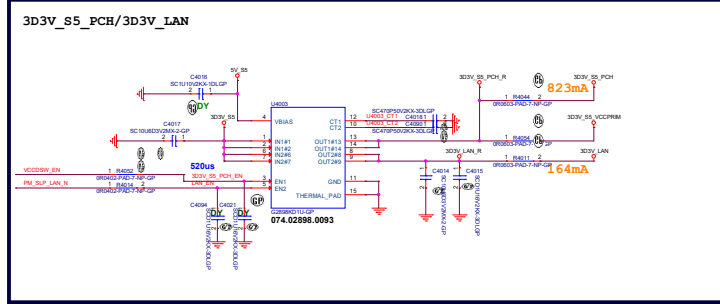
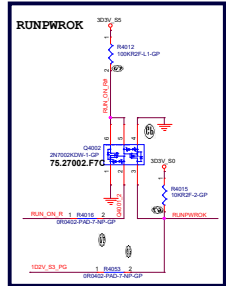
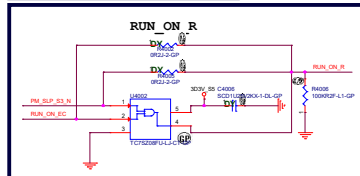
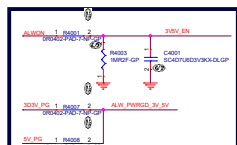
182458 PM_SLP_S3_N >>>
24 RUN_ON_EC >>>
24 RUNWROK <<<
24 EC_TOUCH_SCREEN_EN >>>
20 PCH_TOUCH_SCREEN_EN >>>
183588 PM_SLP_S3_N >>>

51 100V_SLP_PG >>>
182458 PM_SLP_S3_N <<<

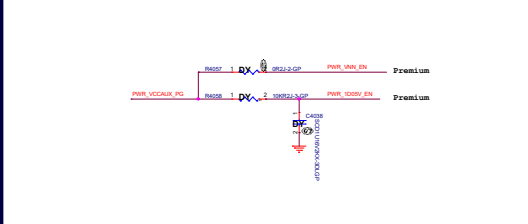
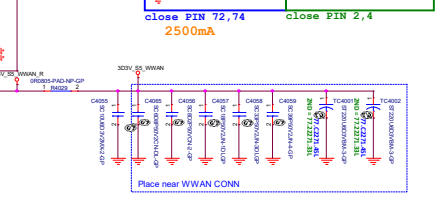
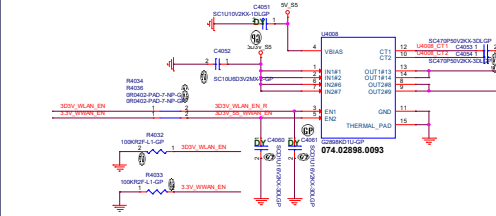
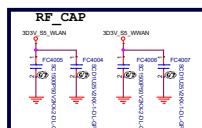
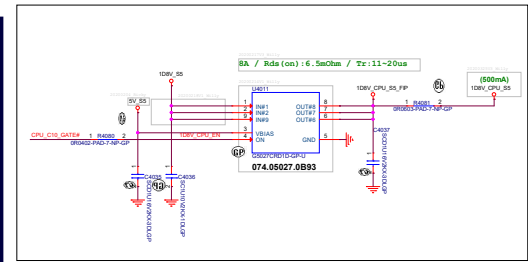
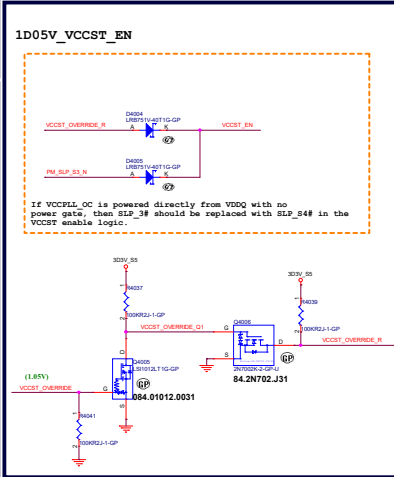
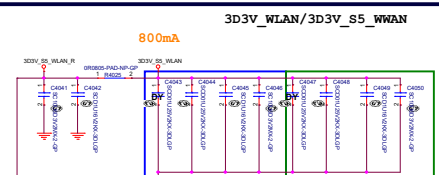
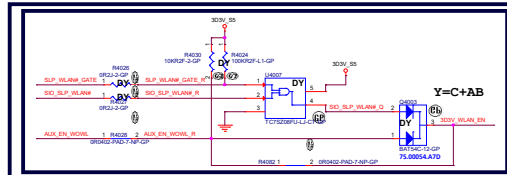
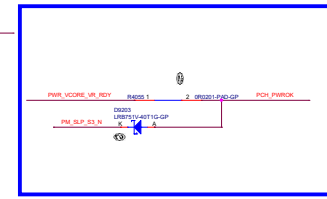
5032 PMW_VCCSTG_PG >>>
54 PMW_100V_EN <<<
54 PMW_100V_EN <<<
622 VCCSTG_OVERHIDE <<<
2453 SLP_PG <<<

54 PMW_UNV100V_PG >>>
1744 PCH_PWDN <<<
PMW_VCCSTG_VN_REV <<<
PMW_VCCSTG_VN_REV <<<
50 XDP_OVERHIDE <<<

??? Not ready
Should confirm with Dell




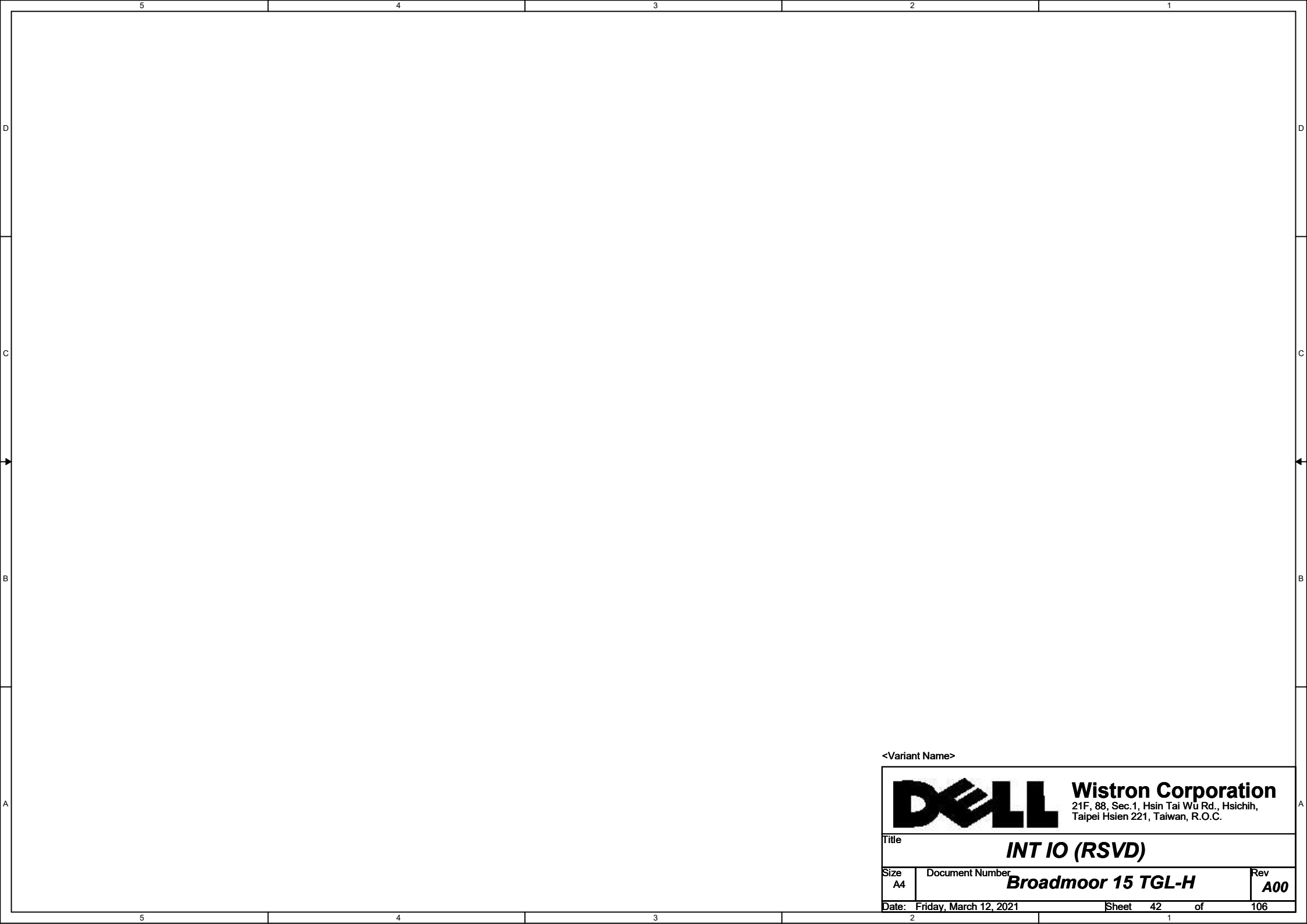
Volume PMW_VCCSTG_PG >>>
Premium PMW_UNV100V_PG >>>
100V_SLP_PG >>>




5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Sequence (RSVD) (DS3/S0ix)					
Size		Document Number			Rev
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<Variant Name>

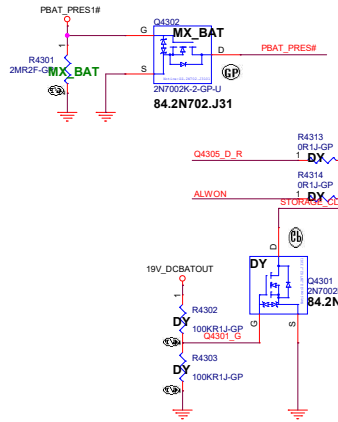
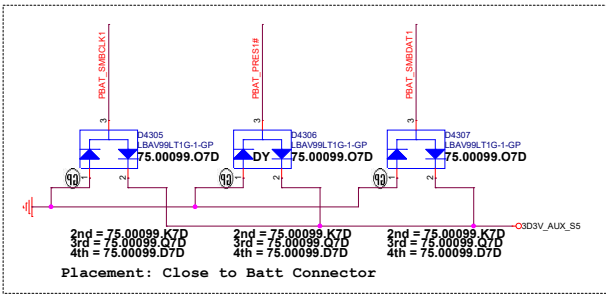
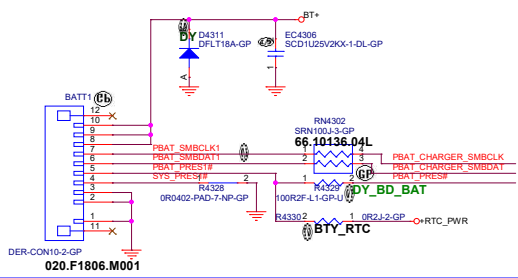
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)			
Size A4	Document Number Broadmoor 15 TGL-H		Rev A00
Date: Friday, March 12, 2021		Sheet 42 of	106

Main Func = BATT Com

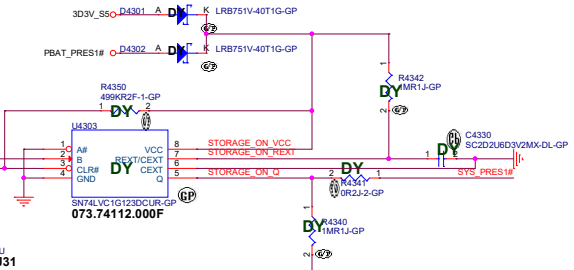
- 24,44 AC_DIS >>>
- 24,44,96 PBAT_CHARGER_SMBCLK <<<
- 24,44,96 PBAT_CHARGER_SMBDAT <<<
- 24,44 PBAT_PRES# <<<
- 24,44,74 AC_DISC# <<<
- 24 POWER_SW_IN# <<<
- 24,40 ALWON >>>
- 96 PBAT_SMBCLK1 >>>
- 96 PBAT_SMBDAT1 >>>

Close BATT1(p.43)

Batt Connector



ADVANCED STORAGE MODE

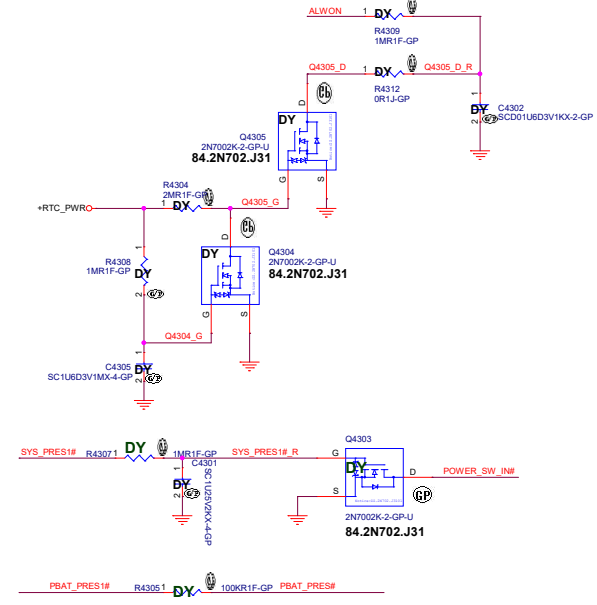


FUNCTION TABLE				
PCB	A	B	OUTPUTS	Q
L	X	X	L	L
X	H	X	L	L
X	X	L	L	L
H	L	T	L	L
H	L	H	L	L
T	L	H	L	L

Normal mode

ADVANCED STORAGE MODE Step1.

Press power button duration time improvement

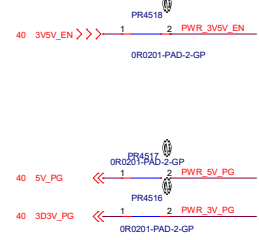


<Variant Name>

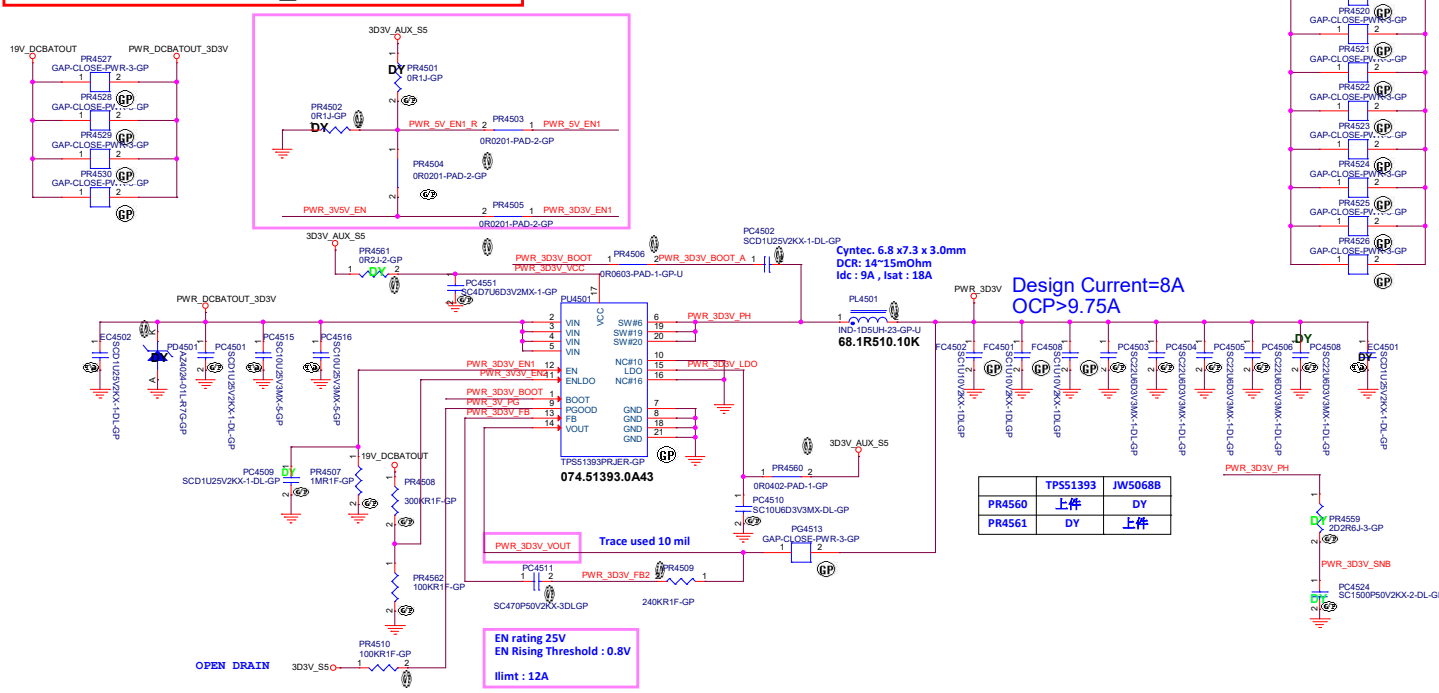
	PR4461	PC4430	PR4447	EC token "SUPPORT_3VLDQ_AS_BATTPRES"
Coin cell battery	DY	Stuff	Stuff	Disable
Battery internal LDO	Stuff	DY	DY	Enable

Location	Gen11	Gen12
PC4451	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PD4425	Stuff	DY
PR4436	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4445	Stuff	DY
PR4452	Stuff	DY
PR4453	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU4415	DY	Stuff
PD4403	DY	Stuff
PD4404	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff
PD4409	Stuff	DY
PR4493	DY	Stuff

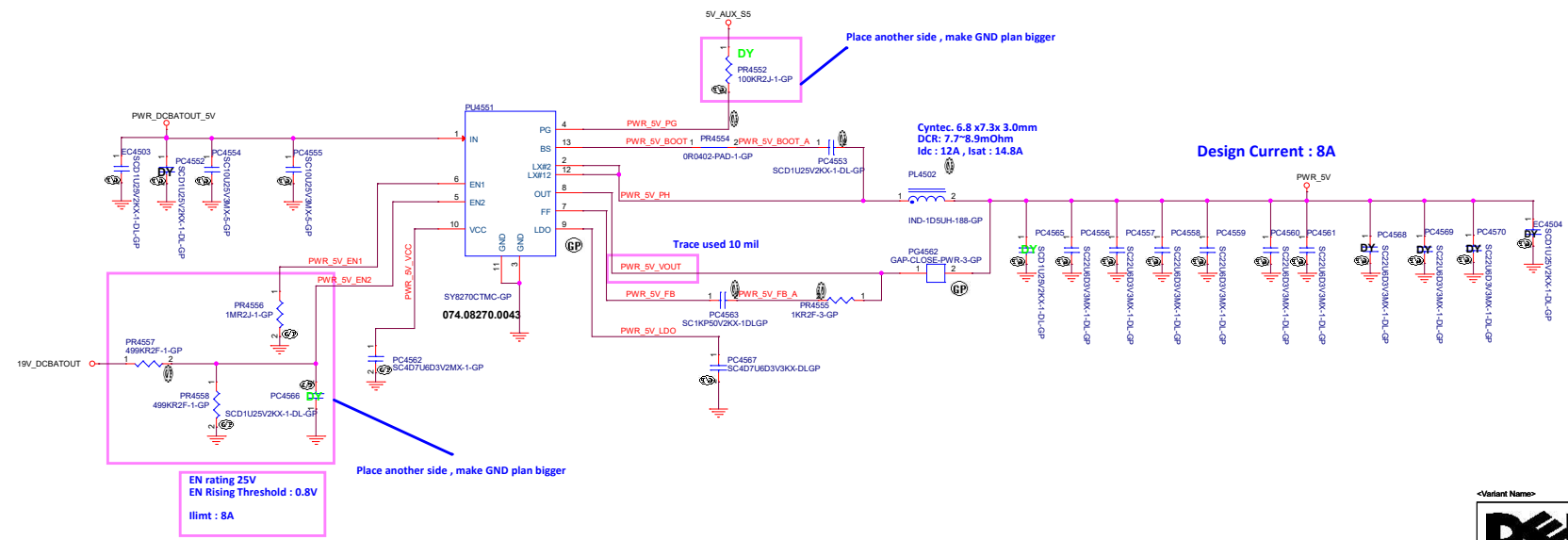
OFFPAGE



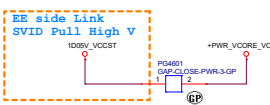
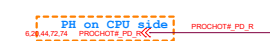
Main Func = Power_System 5V/3D3V



SY8270C For 5V



6 SVID_DATA_CPU >>> SVID_DATA_CPU
6 SVID_CLK_CPU >>> SVID_CLK_CPU
6 SVID_ALERT#_CPU >>> SVID_ALERT#_CPU



Tigerlake IMVP9 Power - H-line 45W 4 phase

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE Impedance=50 Ohm
3. Length match=25mil

Need to Check Net name

PUT CLOSE TO VCORE MOSFET HOT SPOT

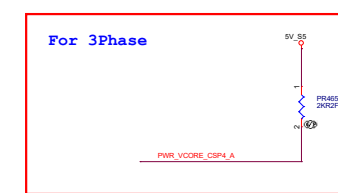
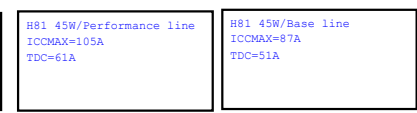
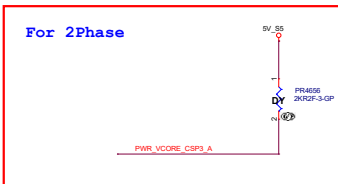
PUT CLOSE TO PWR SC10U18V2KX-1D.GP

H81 45W, ICCMAX=1, TDC=61A

BOTTOM PAD CONNECT TO GND through 5 Vias

Component Values:

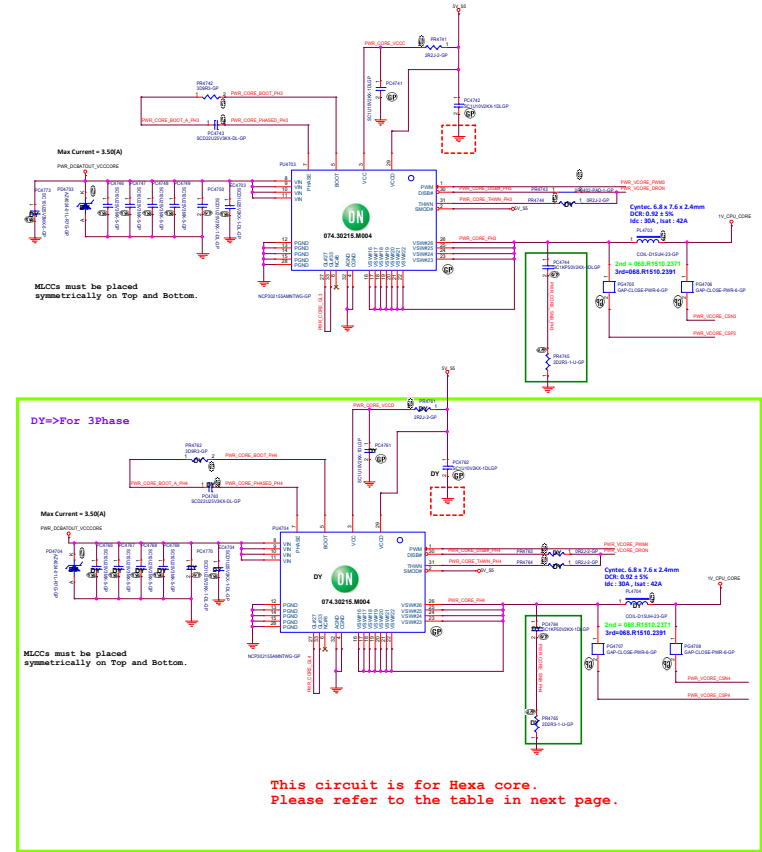
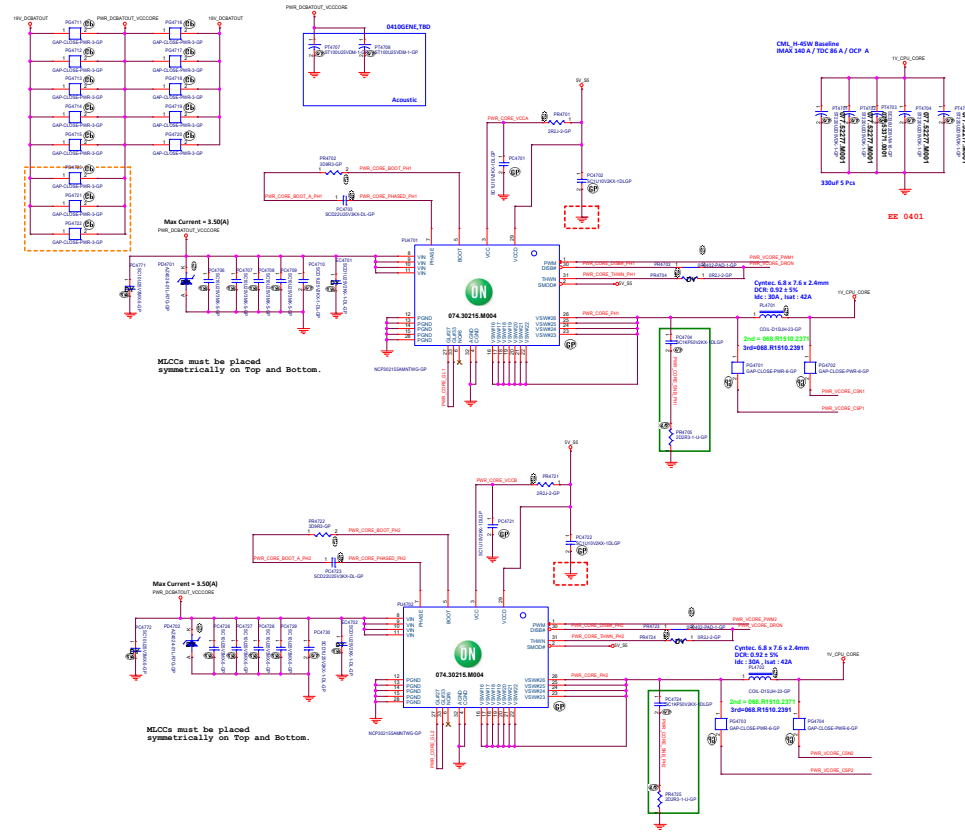
Component	Value
P0C1	100K-12-GP-U
P0C2	100K-12-GP-U
P0C3	100K-12-GP-U
P0C4	100K-12-GP-U
P0C5	100K-12-GP-U
P0C6	100K-12-GP-U
P0C7	100K-12-GP-U
P0C8	100K-12-GP-U
P0C9	100K-12-GP-U
P0C10	100K-12-GP-U
P0C11	100K-12-GP-U
P0C12	100K-12-GP-U
P0C13	100K-12-GP-U
P0C14	100K-12-GP-U
P0C15	100K-12-GP-U
P0C16	100K-12-GP-U
P0C17	100K-12-GP-U
P0C18	100K-12-GP-U
P0C19	100K-12-GP-U
P0C20	100K-12-GP-U
P0C21	100K-12-GP-U
P0C22	100K-12-GP-U
P0C23	100K-12-GP-U
P0C24	100K-12-GP-U
P0C25	100K-12-GP-U
P0C26	100K-12-GP-U
P0C27	100K-12-GP-U
P0C28	100K-12-GP-U
P0C29	100K-12-GP-U
P0C30	100K-12-GP-U
P0C31	100K-12-GP-U
P0C32	100K-12-GP-U
P0C33	100K-12-GP-U
P0C34	100K-12-GP-U
P0C35	100K-12-GP-U
P0C36	100K-12-GP-U
P0C37	100K-12-GP-U
P0C38	100K-12-GP-U
P0C39	100K-12-GP-U
P0C40	100K-12-GP-U
P0C41	100K-12-GP-U
P0C42	100K-12-GP-U
P0C43	100K-12-GP-U
P0C44	100K-12-GP-U
P0C45	100K-12-GP-U
P0C46	100K-12-GP-U
P0C47	100K-12-GP-U
P0C48	100K-12-GP-U
P0C49	100K-12-GP-U
P0C50	100K-12-GP-U
P0C51	100K-12-GP-U
P0C52	100K-12-GP-U
P0C53	100K-12-GP-U
P0C54	100K-12-GP-U
P0C55	100K-12-GP-U
P0C56	100K-12-GP-U
P0C57	100K-12-GP-U
P0C58	100K-12-GP-U
P0C59	100K-12-GP-U
P0C60	100K-12-GP-U
P0C61	100K-12-GP-U
P0C62	100K-12-GP-U
P0C63	100K-12-GP-U
P0C64	100K-12-GP-U
P0C65	100K-12-GP-U
P0C66	100K-12-GP-U
P0C67	100K-12-GP-U
P0C68	100K-12-GP-U
P0C69	100K-12-GP-U
P0C70	100K-12-GP-U
P0C71	100K-12-GP-U
P0C72	100K-12-GP-U
P0C73	100K-12-GP-U
P0C74	100K-12-GP-U
P0C75	100K-12-GP-U
P0C76	100K-12-GP-U
P0C77	100K-12-GP-U
P0C78	100K-12-GP-U
P0C79	

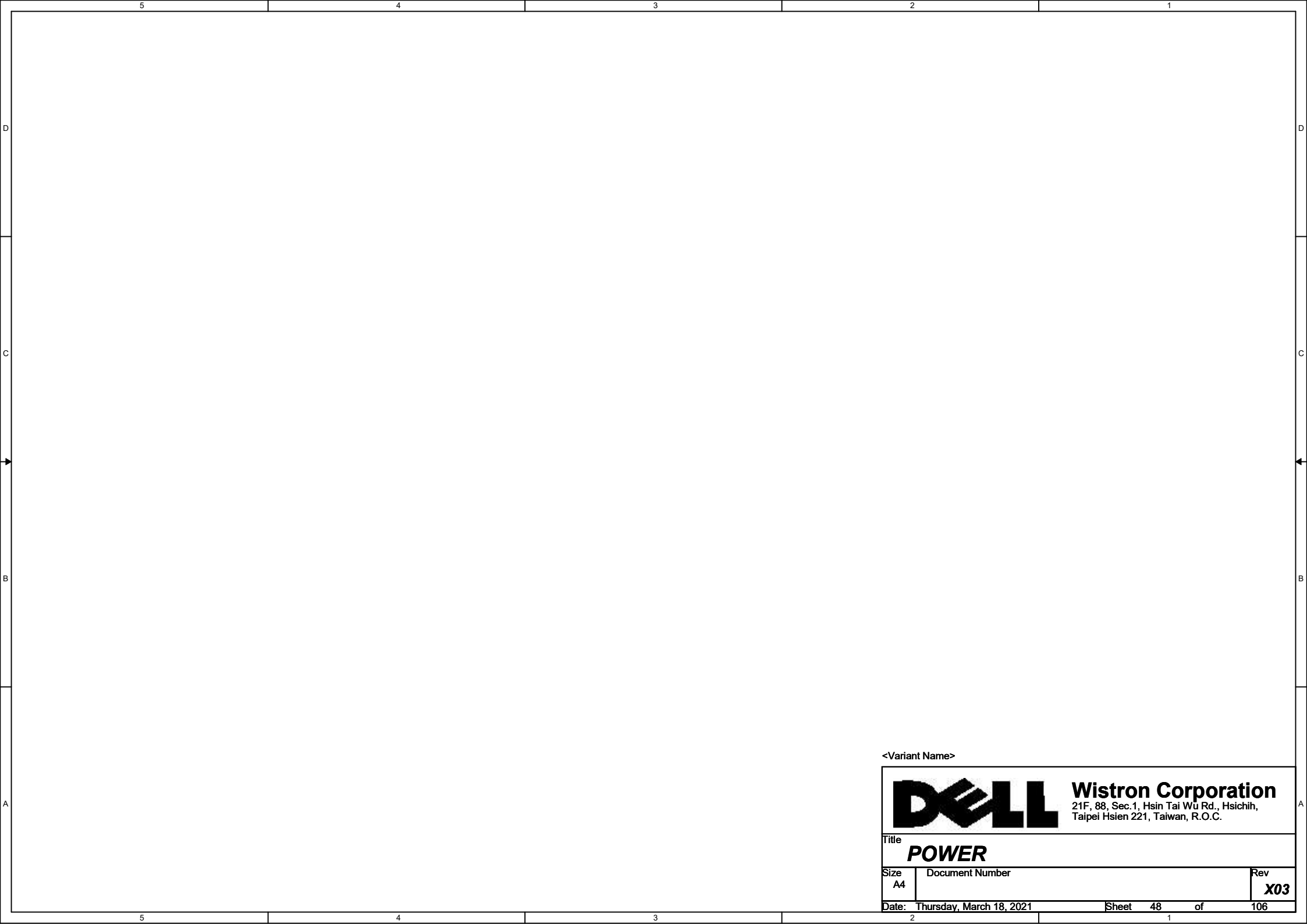


OFFPAGE


4# PWR_VCORE_0R00 → PWR_VCORE_0R00
4# PWR_VCORE_0R01 → PWR_VCORE_0R01
4# PWR_VCORE_0R02 → PWR_VCORE_0R02
4# PWR_VCORE_0R03 → PWR_VCORE_0R03
4# PWR_VCORE_0R04 → PWR_VCORE_0R04

4# PWR_VCORE_0R05 → PWR_VCORE_0R05
4# PWR_VCORE_0R06 → PWR_VCORE_0R06
4# PWR_VCORE_0R07 → PWR_VCORE_0R07
4# PWR_VCORE_0R08 → PWR_VCORE_0R08
4# PWR_VCORE_0R09 → PWR_VCORE_0R09
4# PWR_VCORE_0R10 → PWR_VCORE_0R10






<Variant Name>

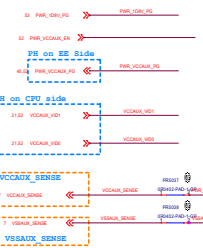
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title POWER		
Size A4	Document Number	Rev X03
Date: Thursday, March 18, 2021		Sheet 48 of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

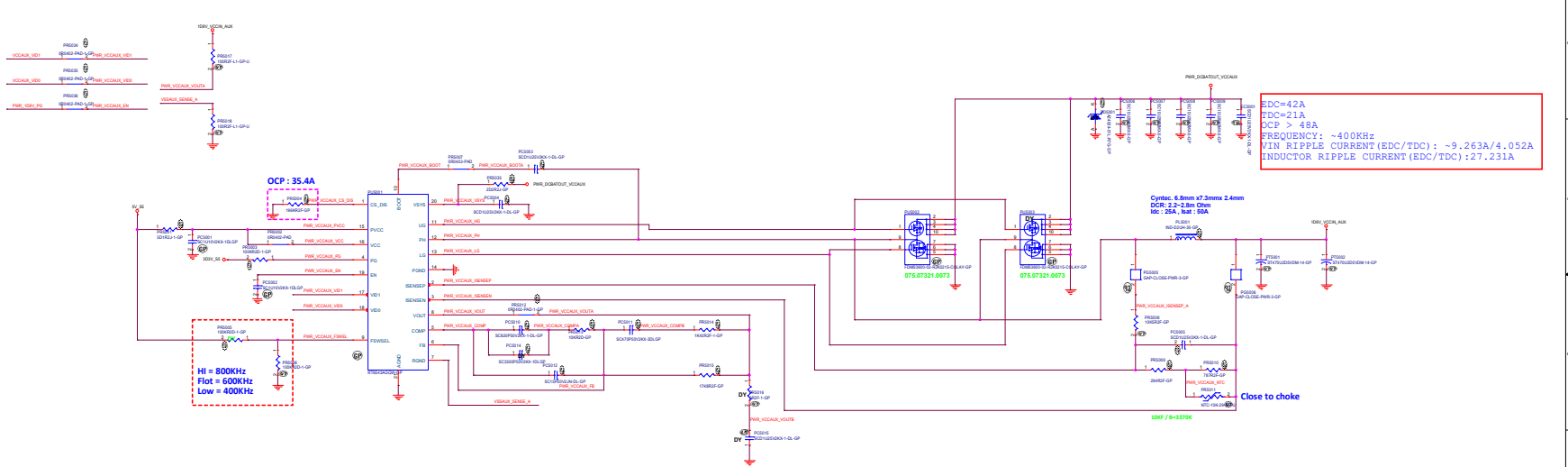
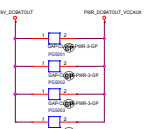
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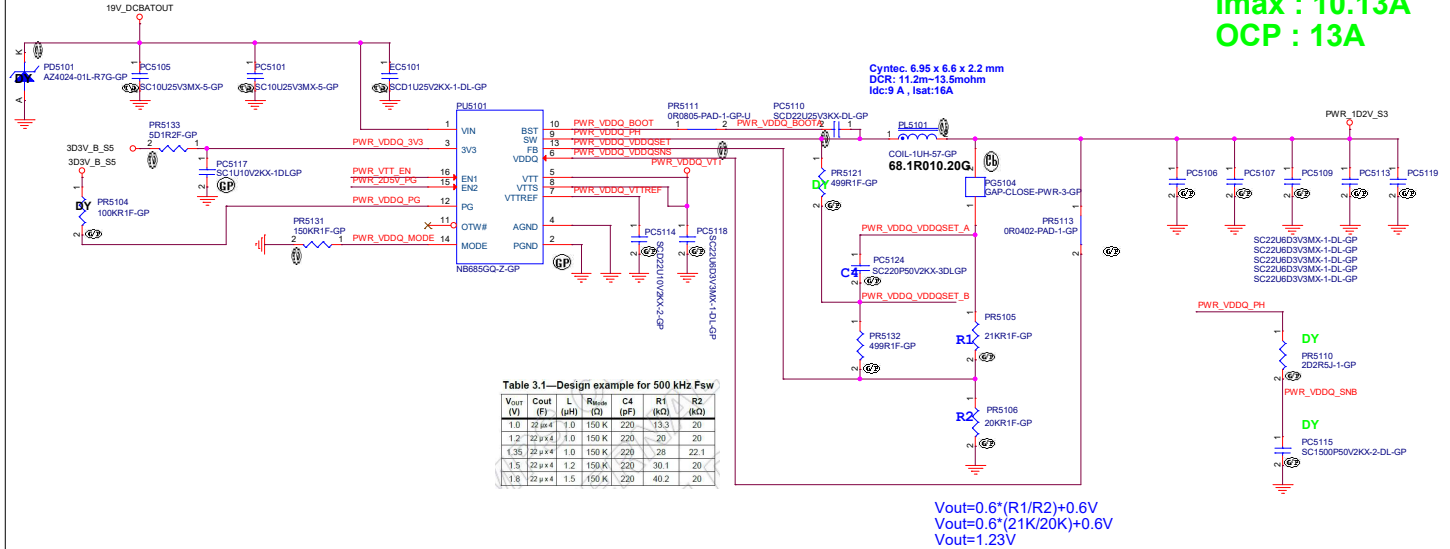
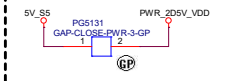
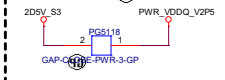
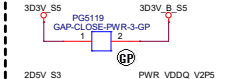
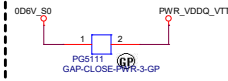
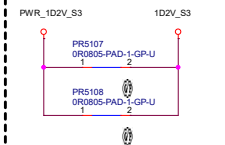
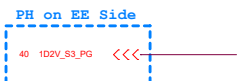
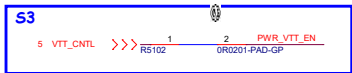
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number	Rev X03
Date: Thursday, March 18, 2021		Sheet 49 of 106

OFFPAGE



OFFPAGE GAP

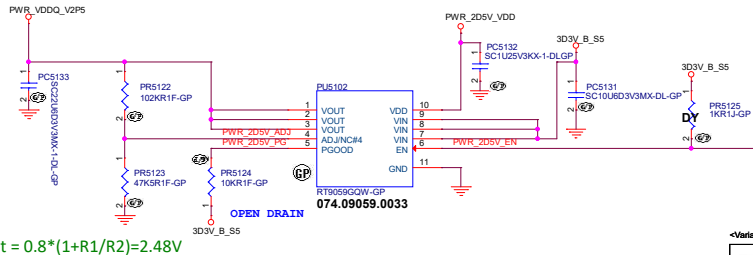




I_{max} : 10.13A
OCP : 13A

Design Current = 0.7A

RT9059GQW for 2D5V

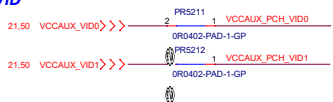


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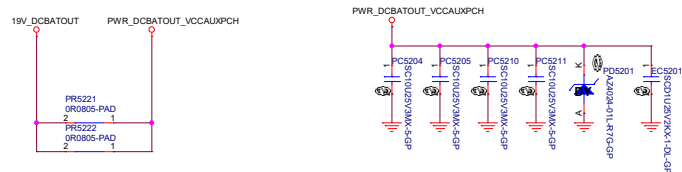
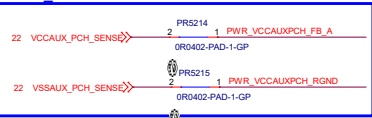
Main Func = VCCIN_AUX

OFFPAGE

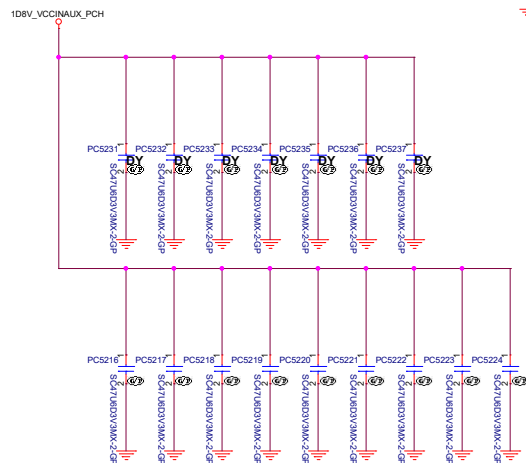
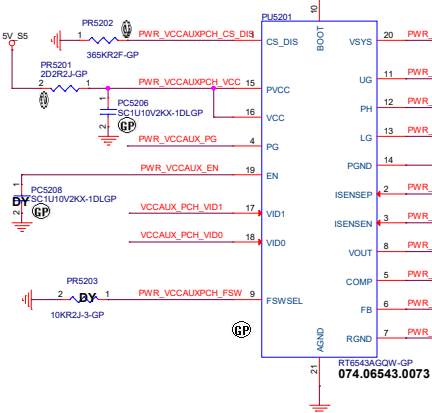
VID



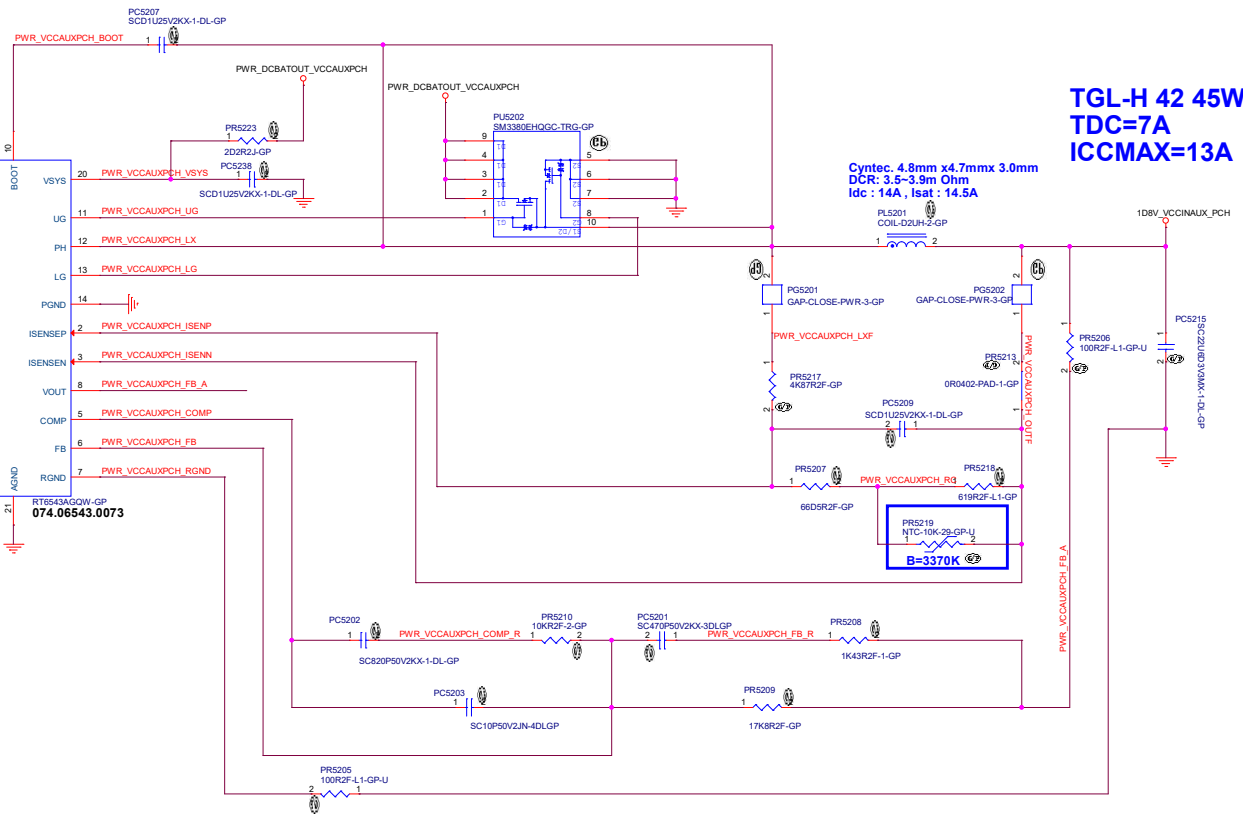
VCCIN_AUX SENSE



OCP=18.2A



Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX_PCH	Primary Side	0603	47uF	5
	Primary Side	0402	10uF	4
	Primary Side	0603	47uF	2



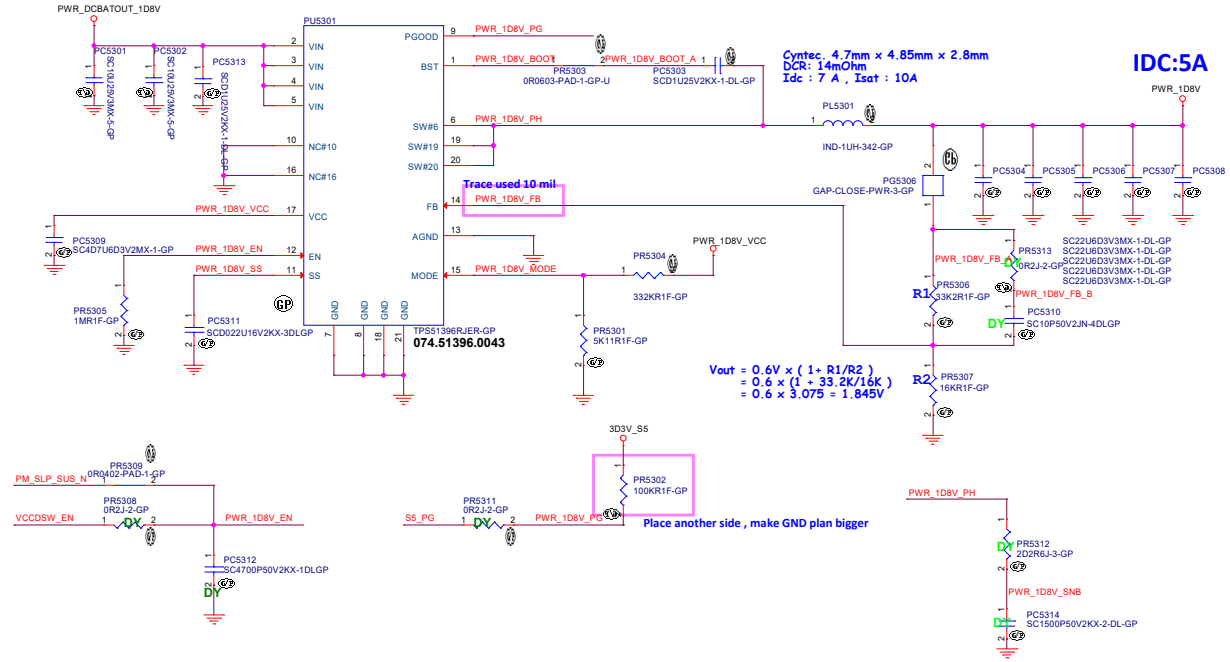
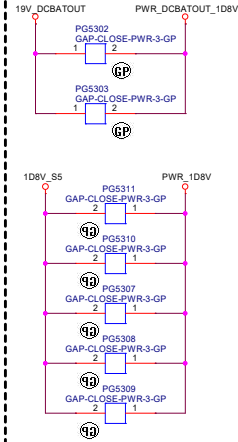
TGL-H 42 45W
TDC=7A
ICCMAX=13A

Cyntec. 4.8mm x4.7mmx 3.0mm
DCR: 3.5~3.9m Ohm
Idc : 14A , Isat : 14.5A

OFFPAGE-Signal

18.24 PM_SLP_SUS_N >>>
24.40 VCCDSW_EN >>>
24.40 SS_PG <<<
50 PWR_1D8V_PG <<<

OFFPAGE-GAP

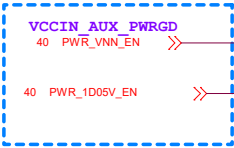


<Variant Name>

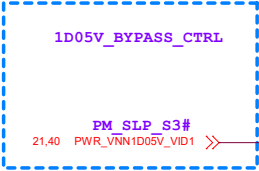
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
file		TPS51396_1D8V	
Size	Document Number	Broadmoor 15 TGL-H	Rev X03
Date:	Thursday, March 18, 2021	Sheet 53 of	106

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PH on EE Side

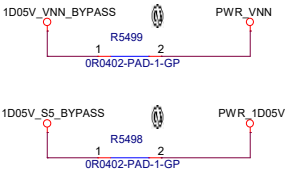


PH on EE Side



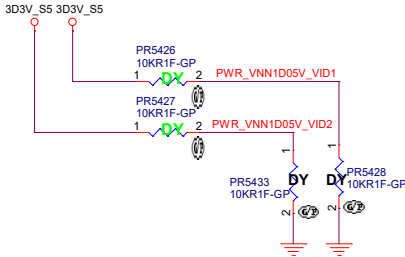
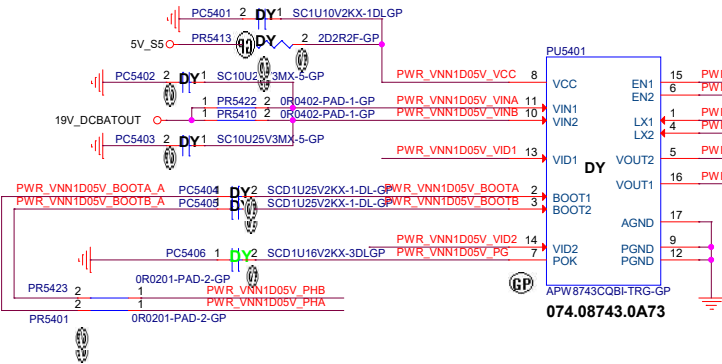
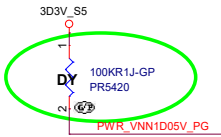
40 PWR_VNN1D05V_PG <<<

OFFPAGE-GAP



VID1 VNN OUTPUT VOLTAGE	
1	0.78 V
0	1.05 V

VID2 V1P05 OUTPUT VOLTAGE	
1	0.96 V
0	1.05 V



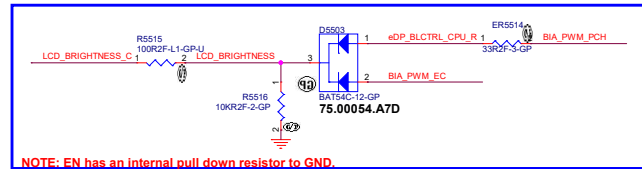
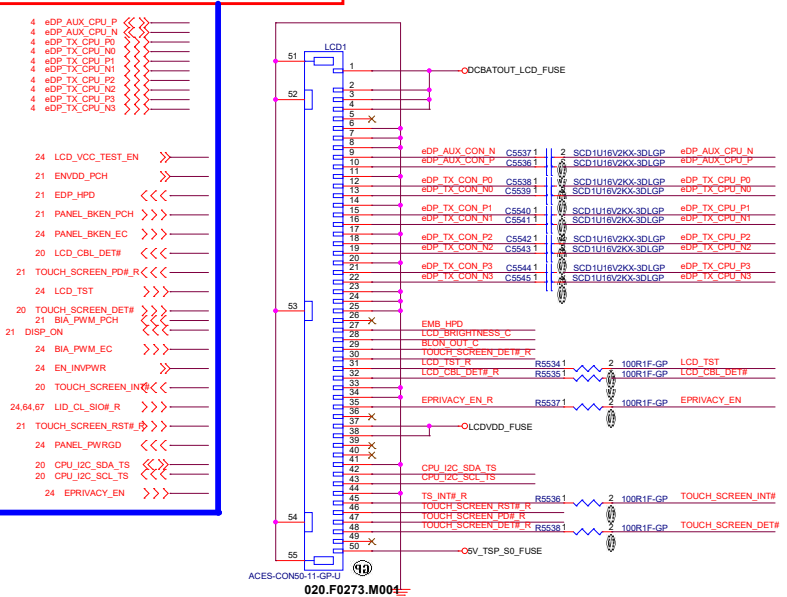
Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A, Isat : 3A

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A, Isat : 1A

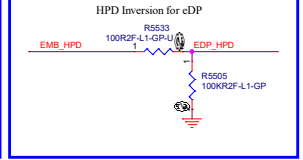
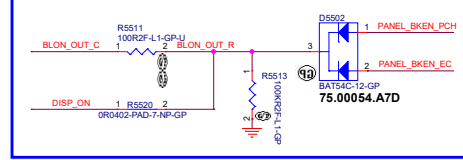
<Variant Name>

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title APW8738_ByPASS		
Size Custom	Document Number	Rev X03
Date: Thursday, March 18, 2021 Sheet 54 of 106		

Main Func = LCD/Touch

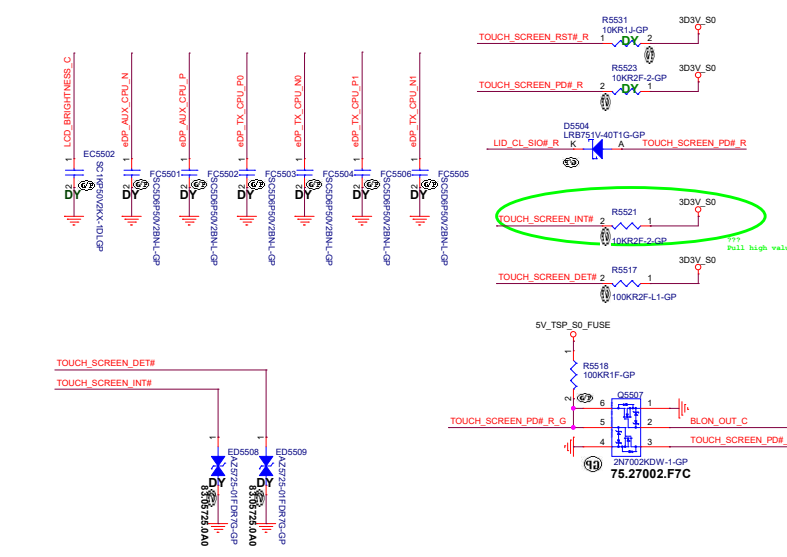
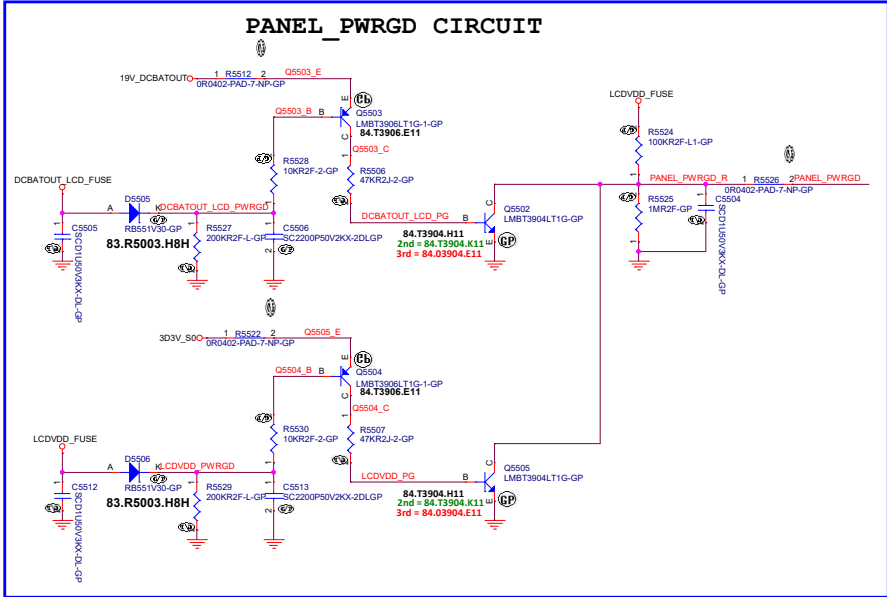
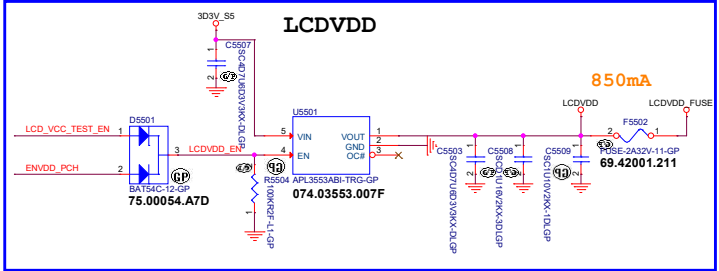
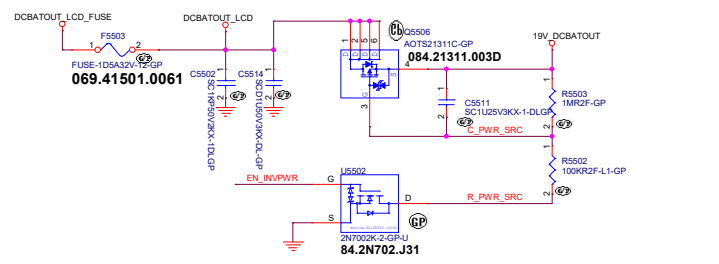


NOTE: EN has an internal pull down resistor to GND.



1086mA

INVERTER POWER



Main Func = IR CAM

18 CCD_USB20_N
18 CCD_USB20_P
27 DMIC_SDA_CODECC
27 DMIC_SCL_CODECC
21 IR_CAM_DET#
20 CAM_MIC_CBL_DET#

21,56,96 P_CLK
21,56,96 P_DATA

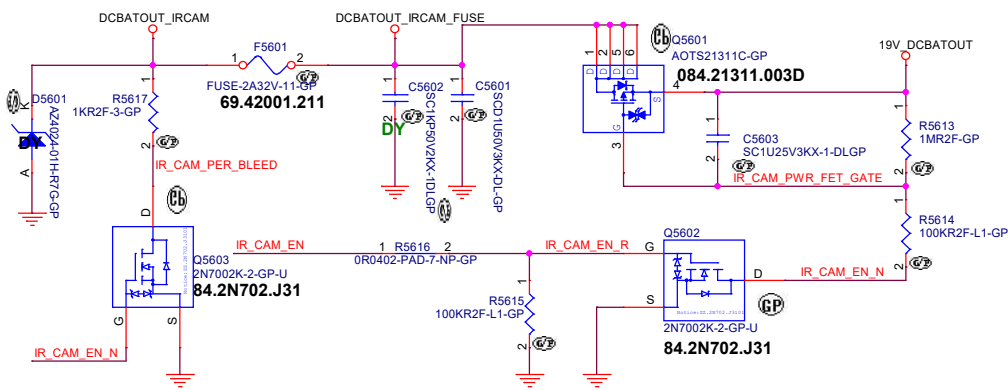
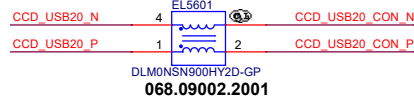
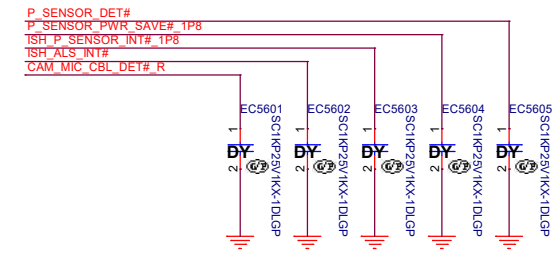
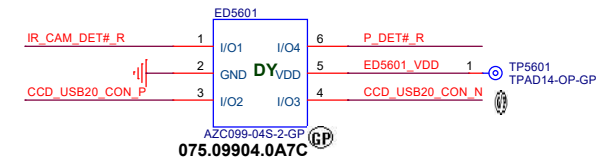
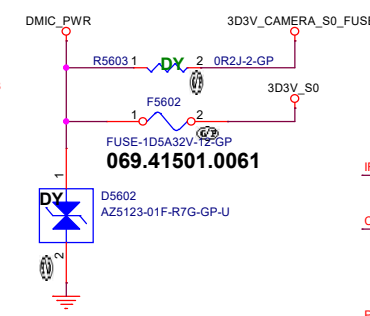
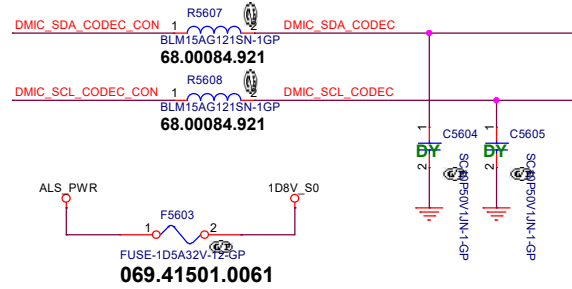
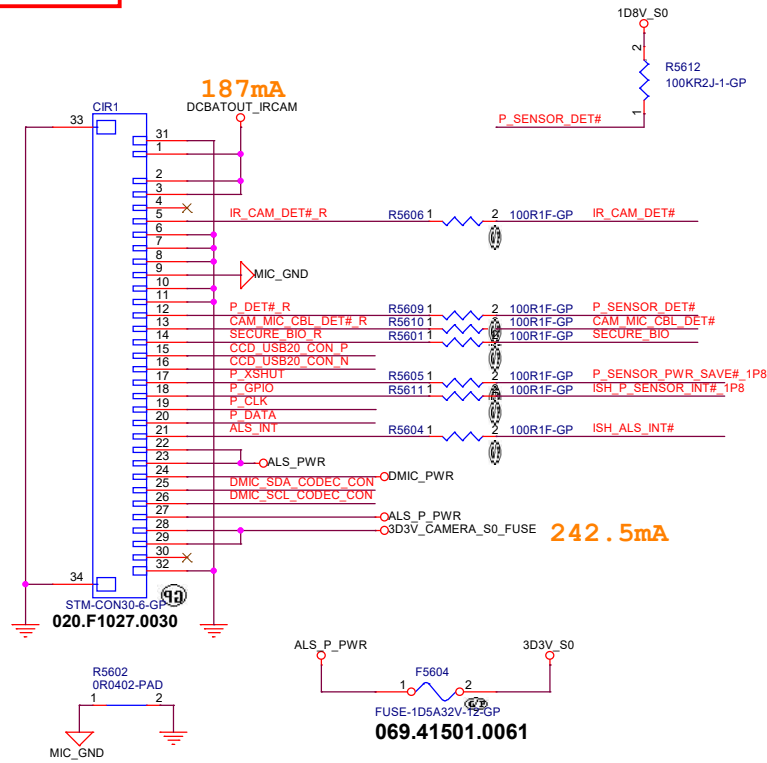
20 P_SENSOR_DET#
21 ISH_ALS_INT#

20 SECURE_BIO
20 P_SENSOR_PWR_SAVE#_1P8

21 ISH_P_SENSOR_INT#_1P8
24 IR_CAM_EN

Close CIR1 (p.56)

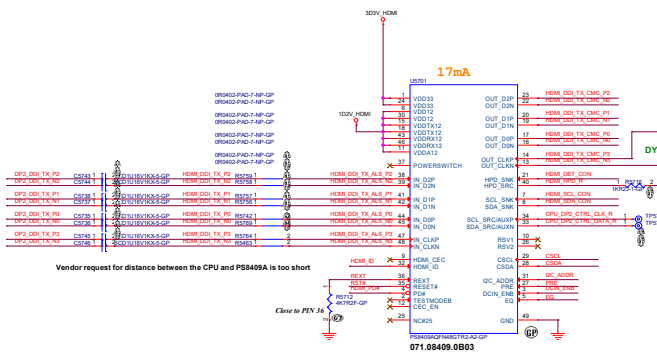
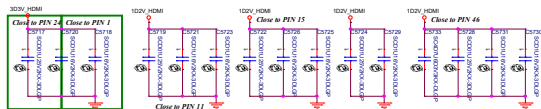
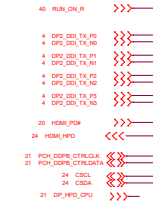
21,56,96 P_CLK
21,56,96 P_DATA



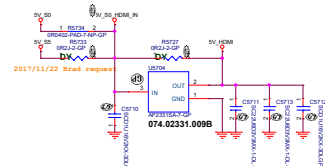
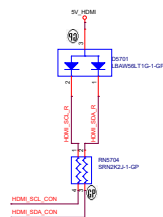
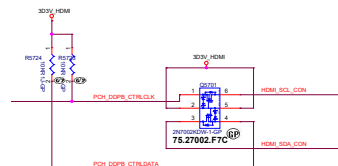
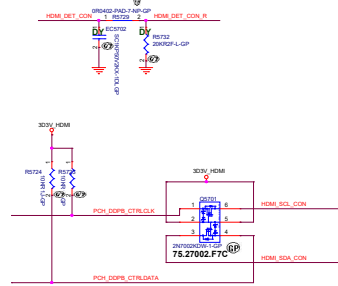
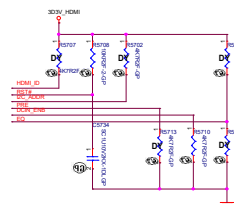
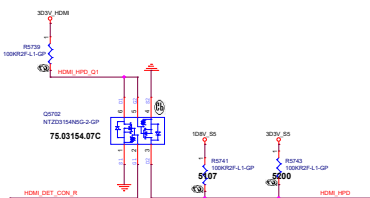
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55 HDMI_SCL_CON
56 HDMI_SDA_CON

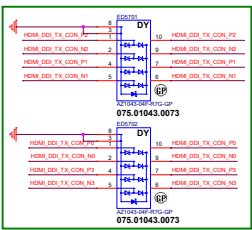
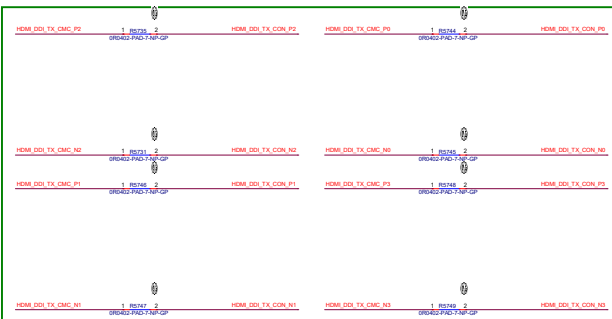
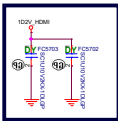
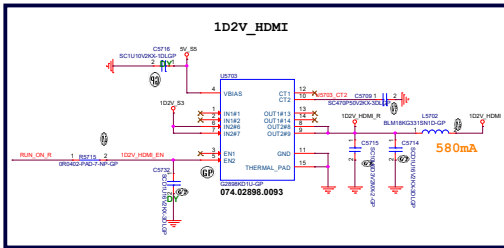
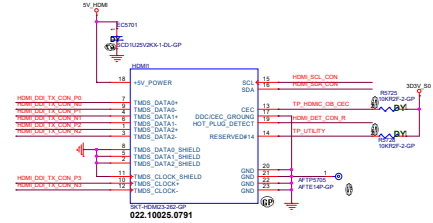
```



Vendor request for distance between the CPU and PS8409A is too short




HDMI CONNECTOR




5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DP			
Size A4	Document Number		Rev A00
Date: Friday, March 12, 2021		Sheet 58 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

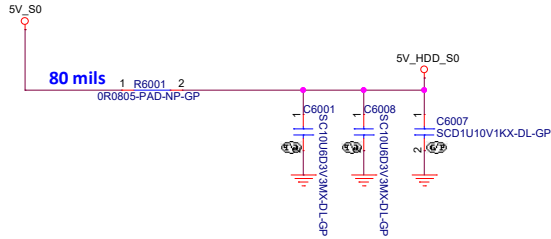
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Display (RSVD) DVI		
Size A4	Document Number	Rev A00
Date: Friday, March 12, 2021		Sheet 59 of 106

SSID = HDD

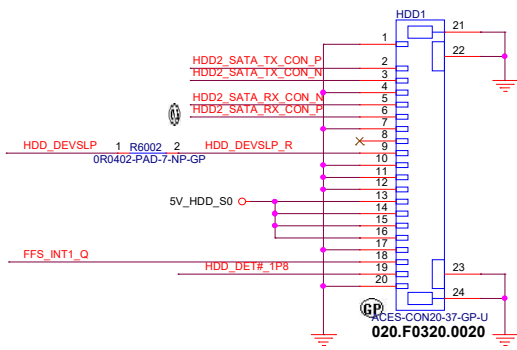
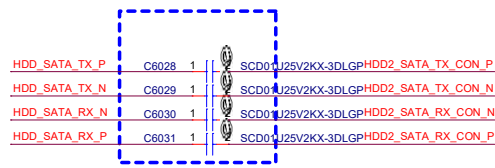
HDD



HDD POWER



SATA HDD Connector



<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

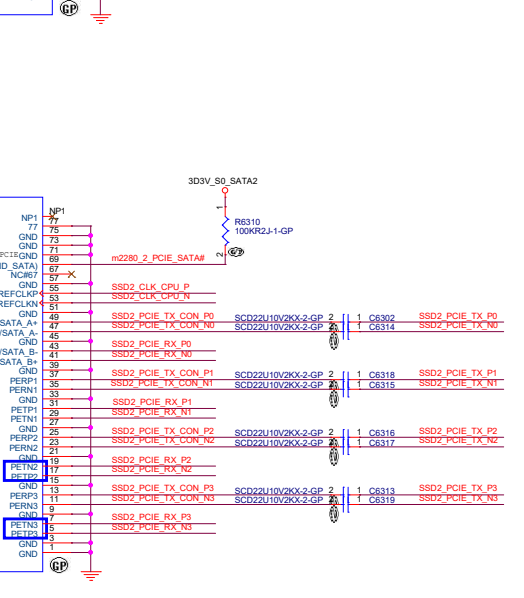
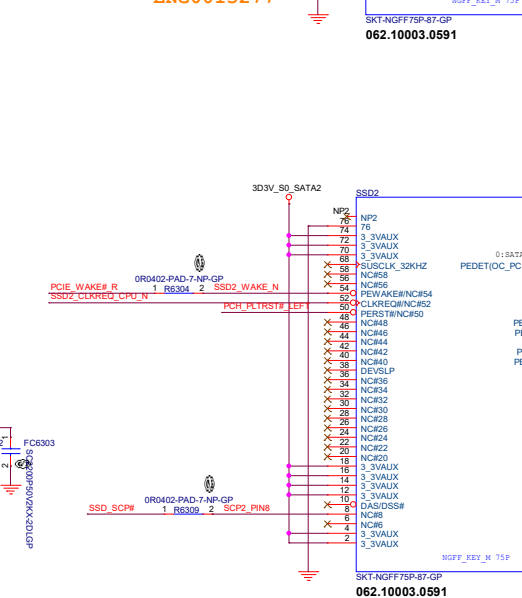
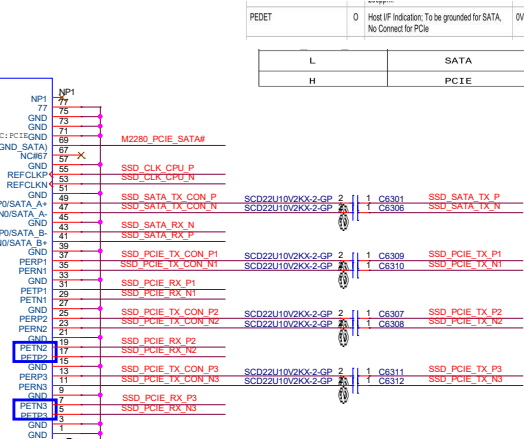
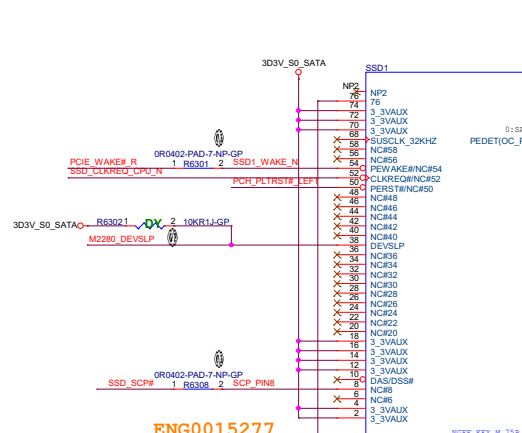
Title **SATA IF HDD/ODD**

Size	Document Number	Rev
Custom	Broadmoor 15 TGL-H	A00
Date: Friday, March 12, 2021	Sheet 60 of 106	

Date: Friday, March 12, 2021 Sheet 61 of 106

PEDET	0	Host I/F Indication: To be grounded for SATA, No Connect for PCIe	0VINC
-------	---	--	-------

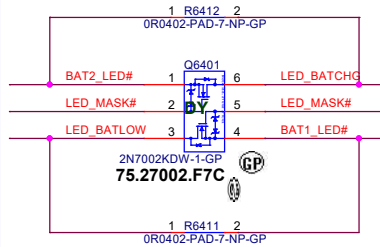
L	SATA
H	PCI-E



<Variant Name>

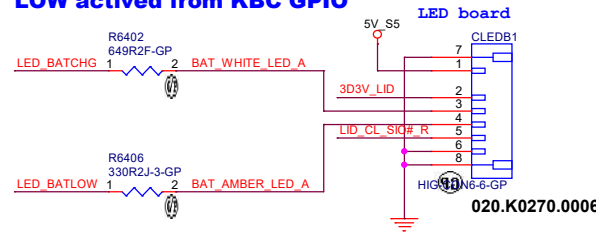
Main Func = LED/HALL/Button

24 BAT2_LED# >>>
24 BAT1_LED# >>>
24,32 LED_MASK# >>>
24,68 KBC_PWRBTN# <<<
24,55,64,67 LID_CL_SIO#_R <<<
92 MASK_BASE_LEDS#_Q <<<
24 POWER_ON_LED# <<<
24,92 FPR_DET# >>>
24 M_BIST >>>
24,44 ACAV_IN >>>
16,17,24,99 RSMRST#_KBC >>>
67 3D3V_LID >>>
24,55,64,67 LID_CL_SIO#_R >>>

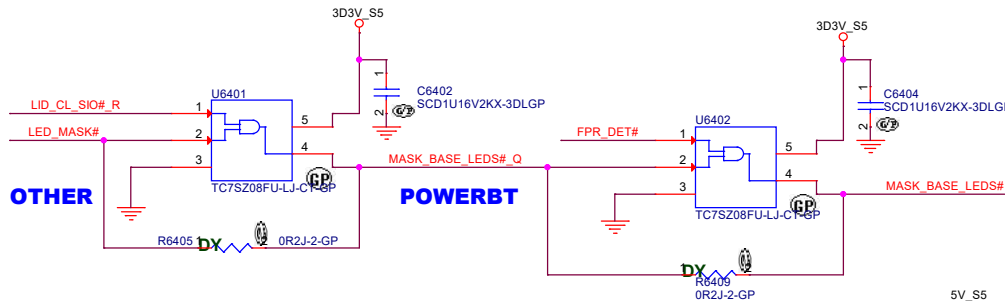
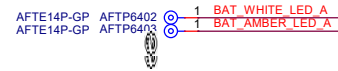


Stealth mode

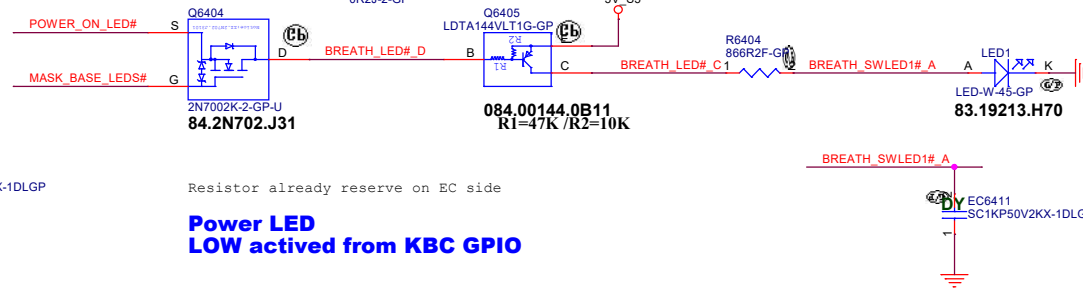
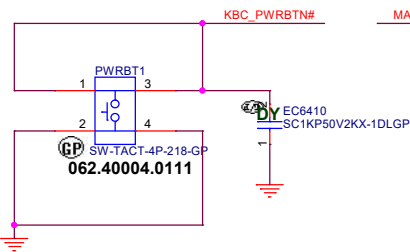
Battery LED2(White LED) LOW activated from KBC GPIO



Battery LED1(Orange LED) LOW activated from KBC GPIO

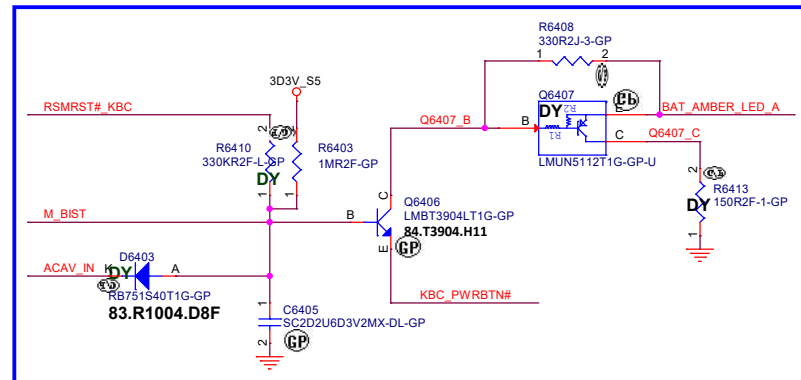


POWER BUTTON



Resistor already reserve on EC side

M-BIST



<Variant Name>

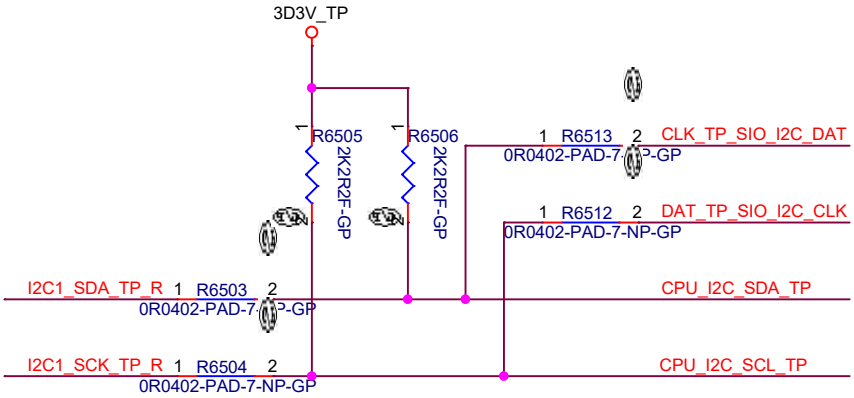
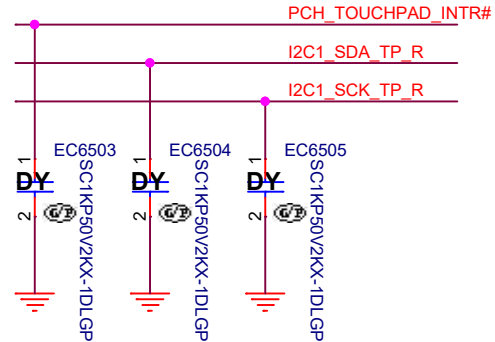
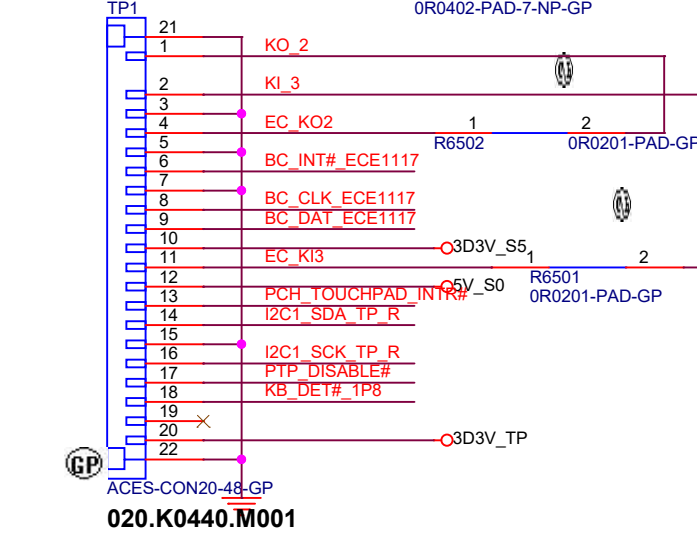
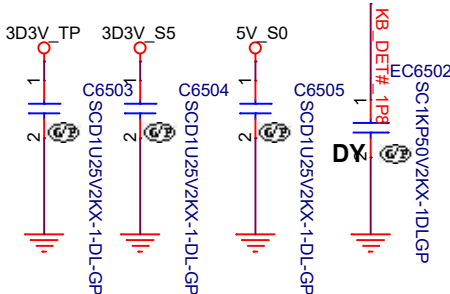
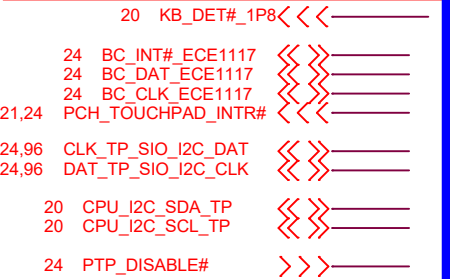
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **LED / Button / Power Button**

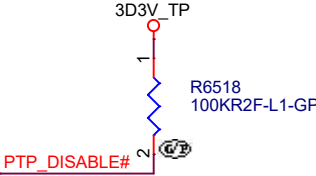
Size Custom Document Number Rev **A00**

Date: Friday, March 12, 2021 Sheet 64 of 106

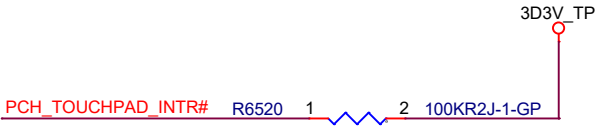
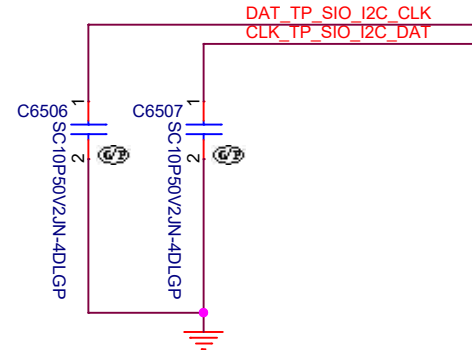
Main Func = Key Board/Touch Pad



10mA



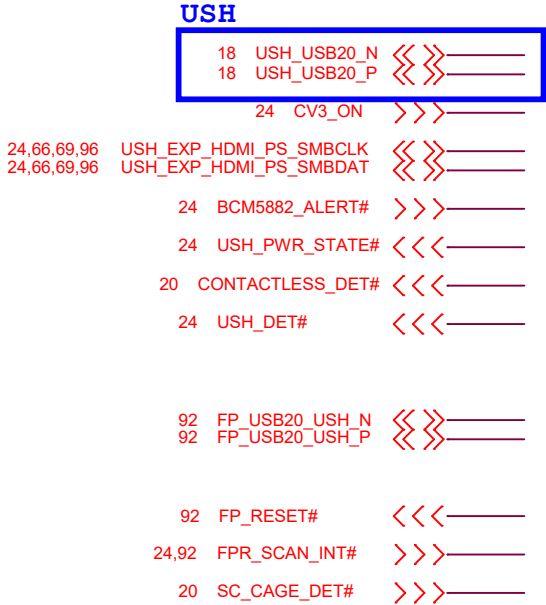
Close TP1 (p.65)



<Variant Name>

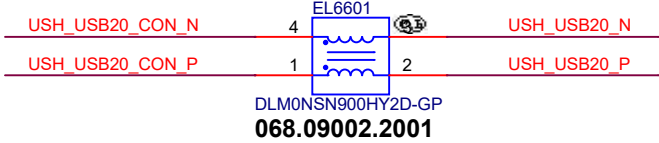
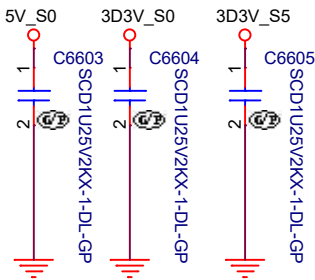
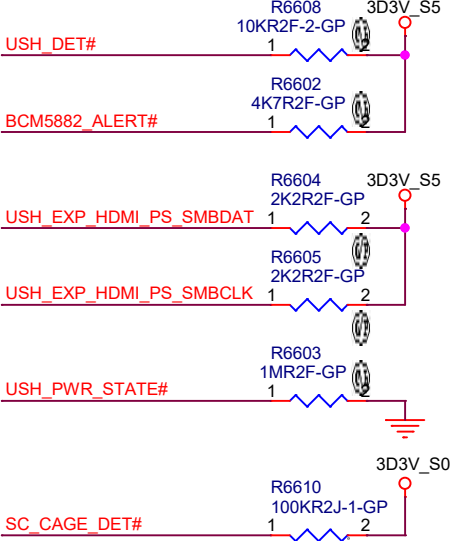
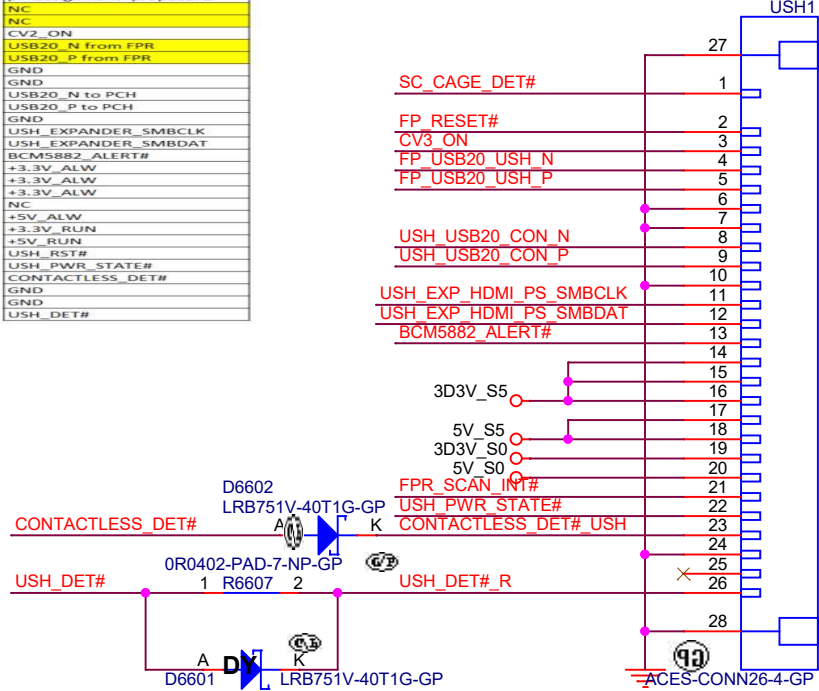
DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (KB/TP)			
Size A4	Document Number		Rev A00
Date: Friday, March 12, 2021		Sheet 65 of	106

Main Func = USH BD



CV3 module
pin assignment - proposal 2

NC
NC
CV2_ON
USB20_N from FPR
USB20_P from FPR
GND
GND
USB20_N to PCH
USB20_P to PCH
GND
USH_EXPANDER_SMBCLK
USH_EXPANDER_SMBDAT
BCM5882_ALERT#
+3.3V_ALW
+3.3V_ALW
+3.3V_ALW
NC
+5V_ALW
+3.3V_RUN
+5V_RUN
USH_RST#
USH_PWR_STATE#
CONTACTLESS_DET#
GND
GND
USH_DET#



Close USH1 (p.66)



<Variant Name>

DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

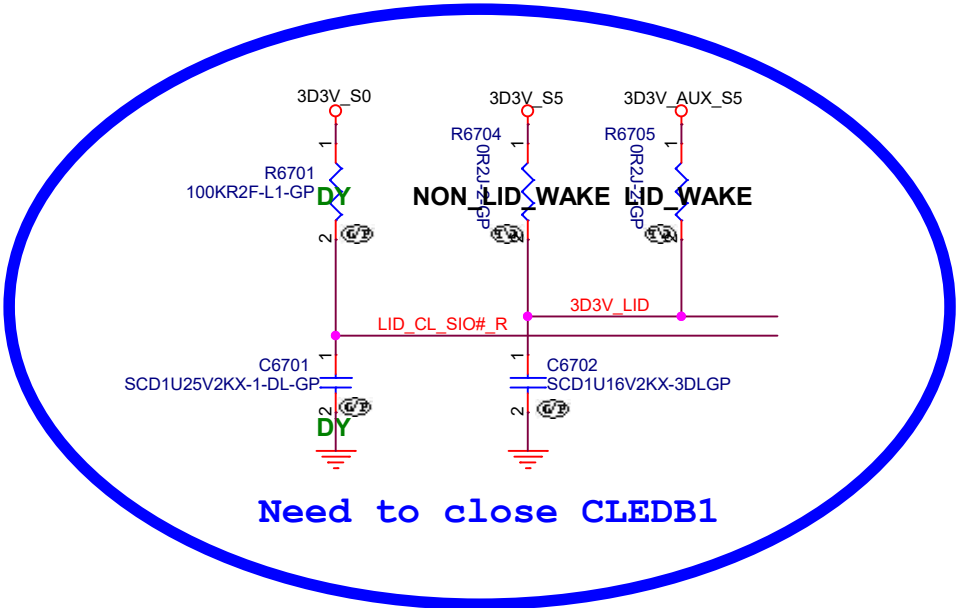
Title
IO Board Conn (USH)

Size A4	Document Number	Rev A00
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Date: Friday, March 12, 2021 Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)

24,55,64 LID_CL_SIO#_R << >>
64 3D3V_LID <<<



<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sensor (Hall-Sensor)			
Size A4	Document Number		Rev A00
Date: Wednesday, March 17, 2021		Sheet 67 of	106

Main Func = Debug

21 ME_FWP_PCH >>>
24 ME_FWP >>>

20 CPU_UART2_TXD >>>
20 CPU_UART2_RXD >>>

16,24,40 PM_SLP_S3_N >>>
16 SIO_SLP_S5# >>>
16,51 PM_SLP_S4_N >>>
16 SIO_SLP_A# >>>
17 RTC_RST_N >>>
24,64 KBC_PWRBTN# >>>
18 SYS_RESET_N >>>
20,91 SIO_SLP_S0# >>>

20,24,96 ESPI_IO0 >>>
20,24,96 ESPI_IO1 >>>
20,24,96 ESPI_IO2 >>>
20,24,96 ESPI_IO3 >>>
20,24,96 ESPI_CS# >>>
20,24 ESPI_RESET# >>>
20,24,96 ESPI_CLK >>>

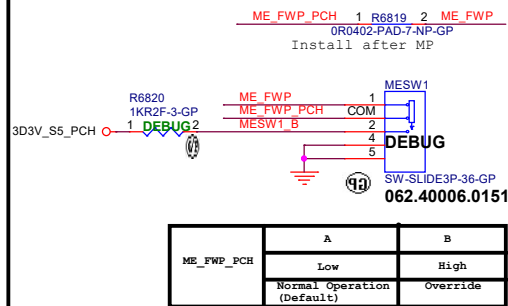
24 JTAG_TDI >>>
24 JTAG_TMS >>>
24 JTAG_CLK >>>
24 JTAG_TDO >>>
24 MSLCK >>>
24 MSDATA >>>
24 HOST_DEBUG_TX >>>
20 SBIOS_TX >>>

24,25,91 SPI_CLK_DEBUG >>>
24,25,91 SPI_SI_DEBUG >>>
24,25,91 SPI_SO_DEBUG >>>
24,25 SPI_WP_DEBUG >>>
24,25 SPI_HOLD_DEBUG >>>
24,25 SPI_CS_DEBUG_N0 >>>
24,25 SPI_CS_DEBUG_N1 >>>

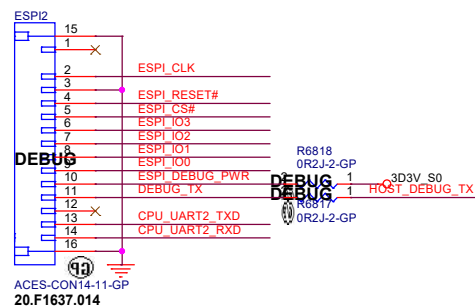
18,96 SPI_CLK_CPU >>>
11,18 SPI_SI_CPU >>>
18,96 SPI_SO_CPU >>>
11,18 SPI_WP_CPU >>>
11,18 SPI_HOLD_CPU >>>
18,96 SPI_CS_CPU_N0 >>>
18 SPI_CS_CPU_N1 >>>

24 PROM_BIOS_R <<<
99 XDP_SPI_WP_CPU >>>

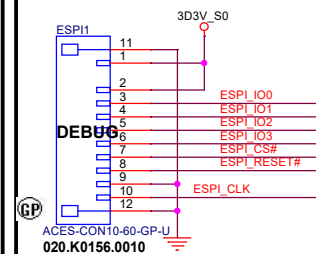
Firmware SW



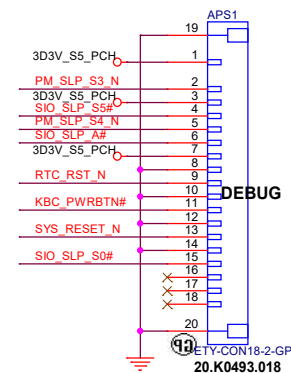
ESPI DEBUG (Wistron)



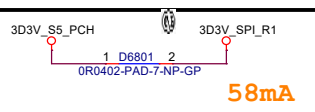
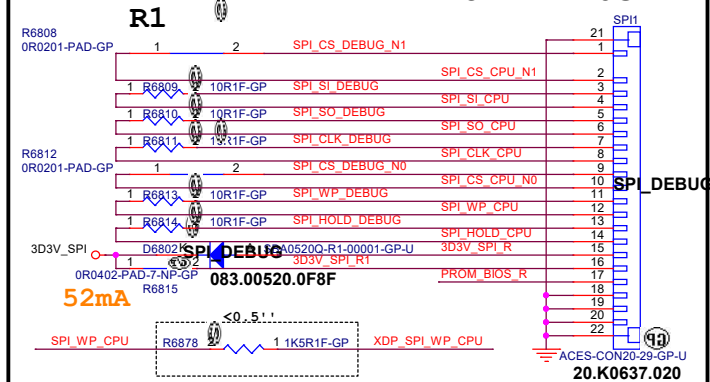
ESPI DEBUG (DELL)



APS DEBUG

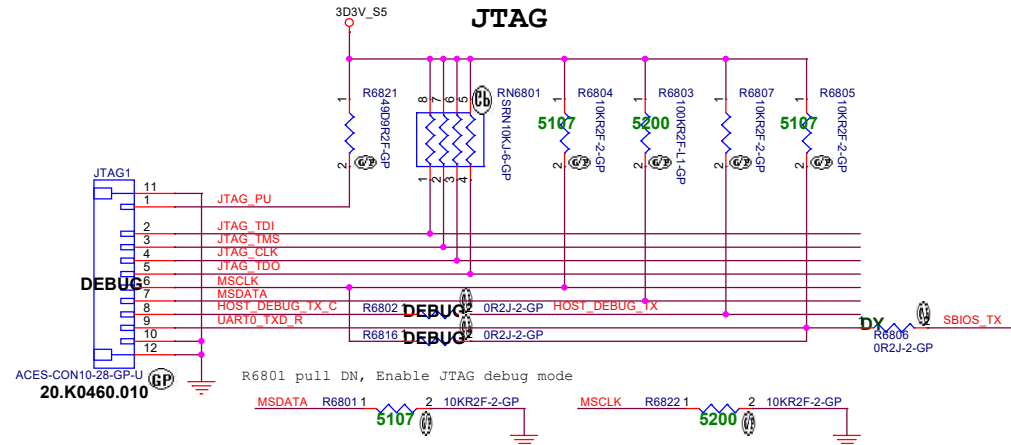


SPI DEBUG



MP change to short pad

JTAG

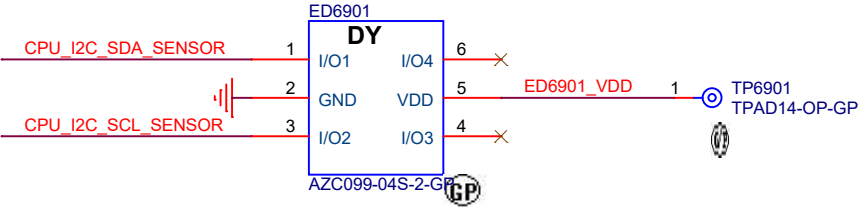
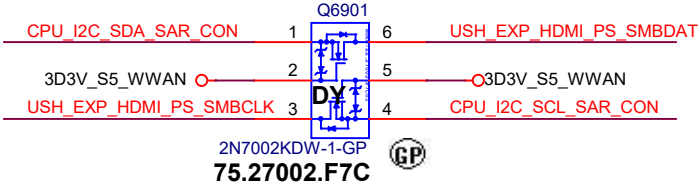
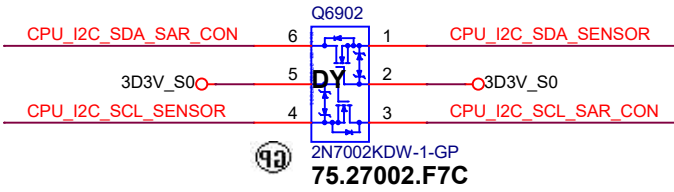
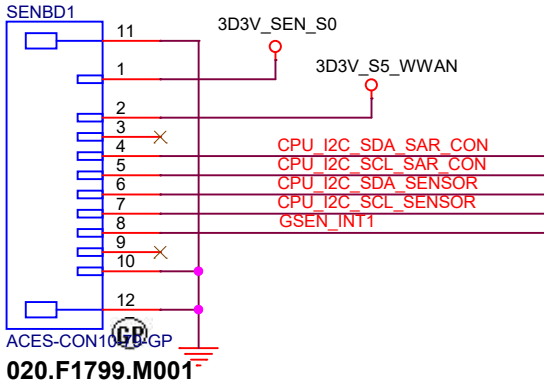
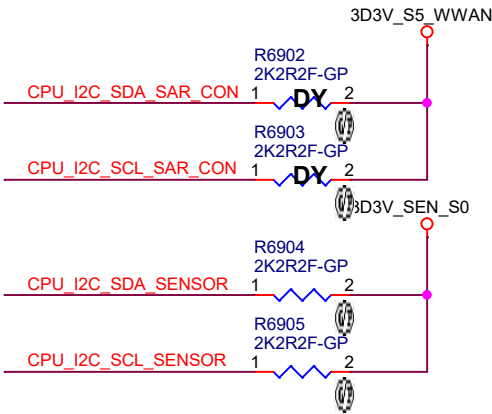
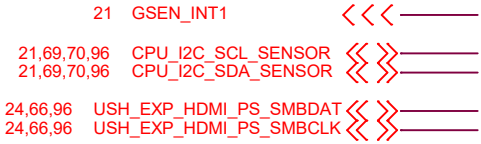


<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Debug (LPC debug)
Size A3 Document Number Rev A00
Date: Friday, March 12, 2021 Sheet 68 of 106


Main Func = Sensor (E-compass/A+Gyro/SAR)



Close SENBD1(p.69)



<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Sensor (GYROSCOPE/PRESSUE/ALS)

Size A4	Document Number	Rev A00
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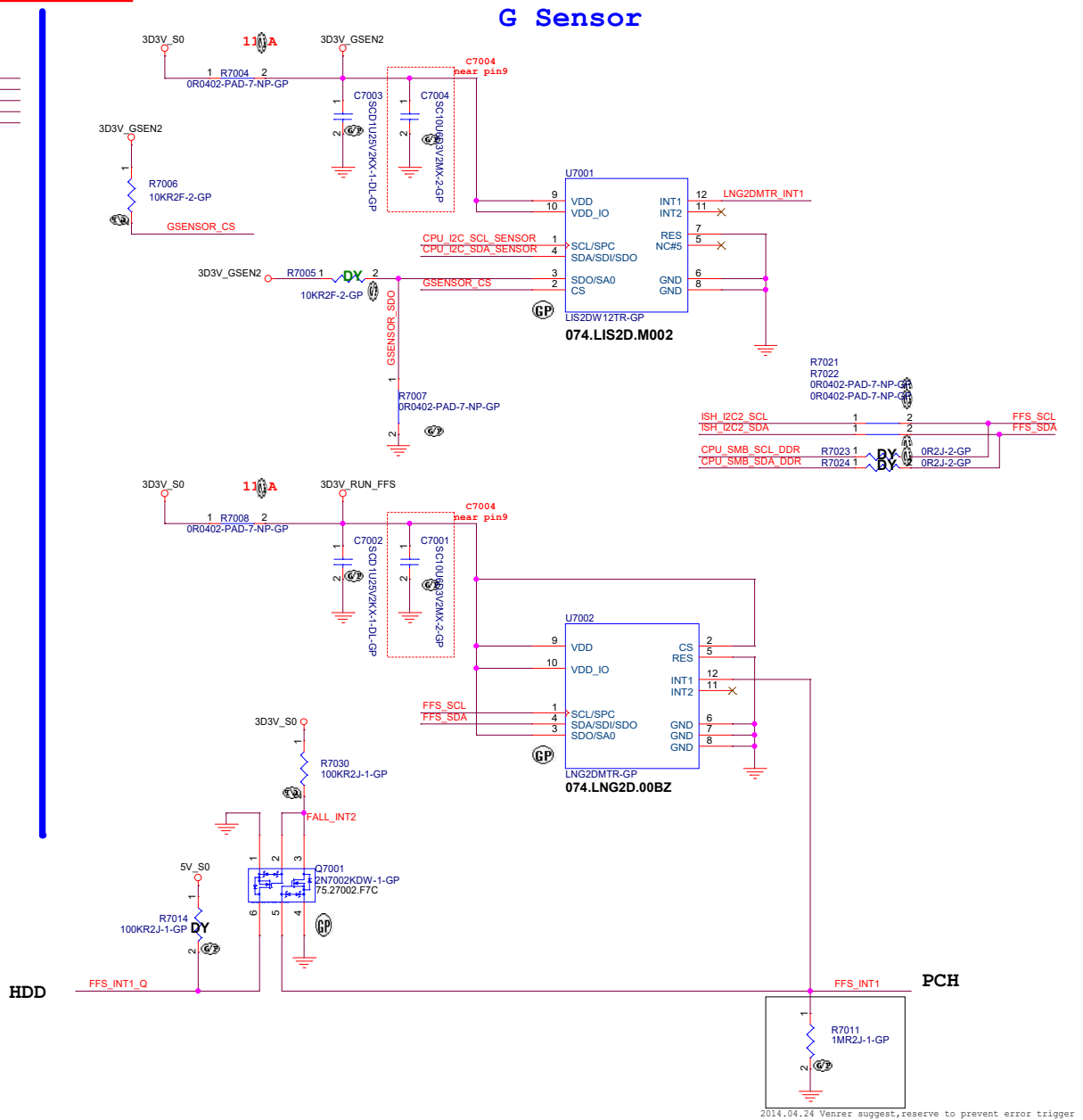
Date: Friday, March 12, 2021 Sheet 69 of 106

Main Func = G-sensor

G Sensor

21,69,70,96 CPU_I2C_SDA_SENSOR
21,69,70,96 CPU_I2C_SCL_SENSOR
21 LNG2DMTR_INT1
60 FFS_INT1_Q
20,21 FFS_INT1
12,13,20,96 CPU_SMB_SCL_DDR
12,13,20,96 CPU_SMB_SDA_DDR
20 ISH_I2C2_SCL
20 ISH_I2C2_SDA
21,69,70,96 CPU_I2C_SCL_SENSOR
21,69,70,96 CPU_I2C_SDA_SENSOR

Close U7001(P.70)

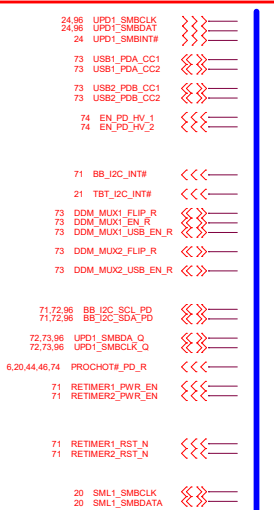


<Variant Name>

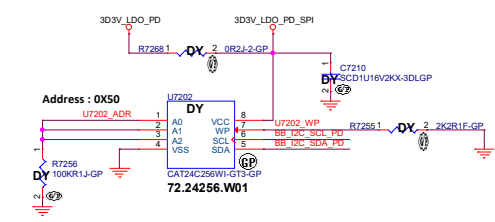
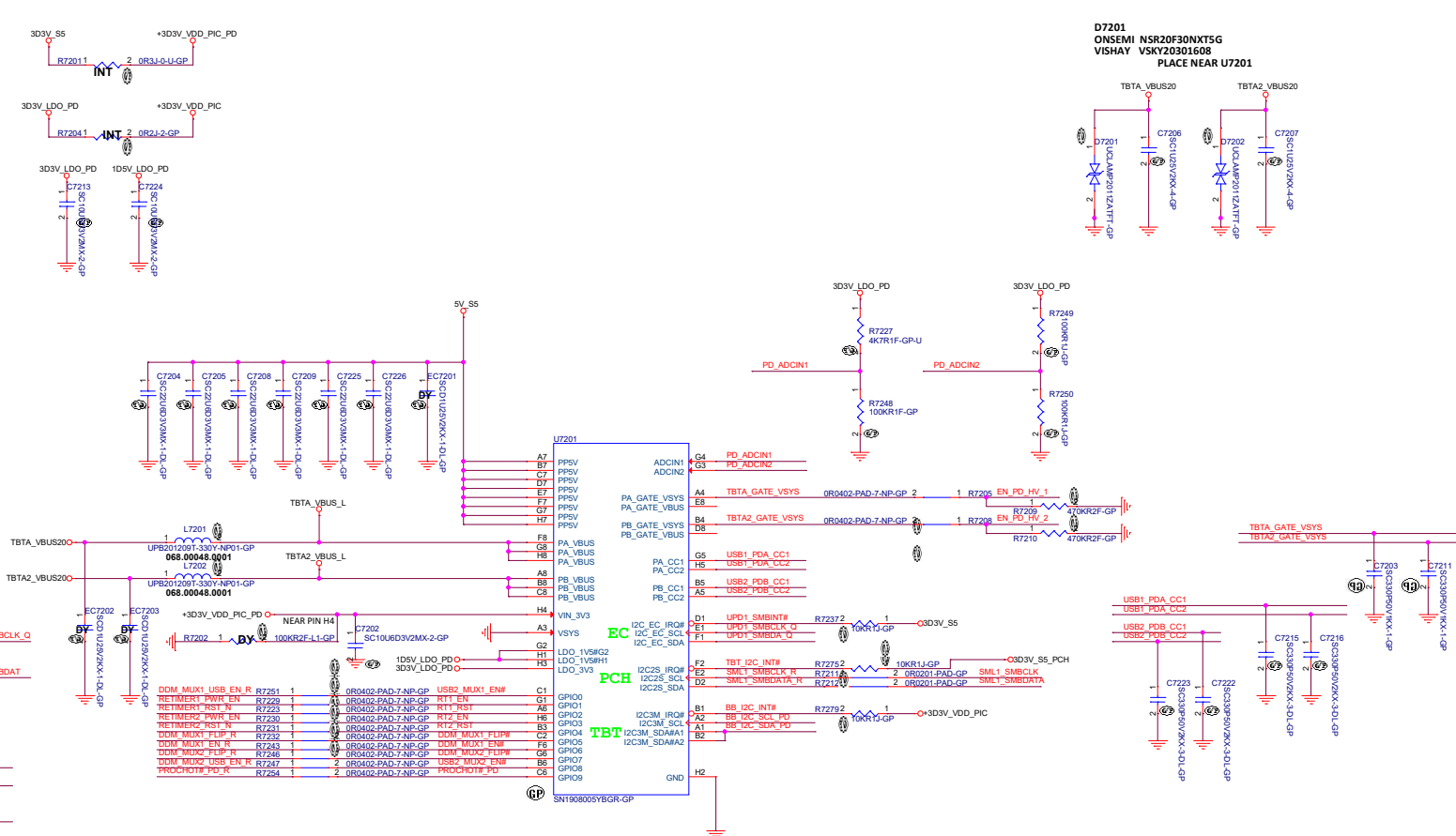
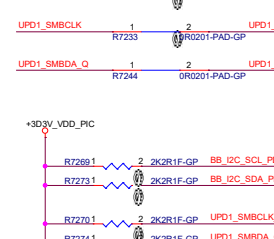
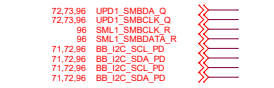
DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Sensor (G-sensor)		
Size Custom	Document Number	Rev A00
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[illegible]

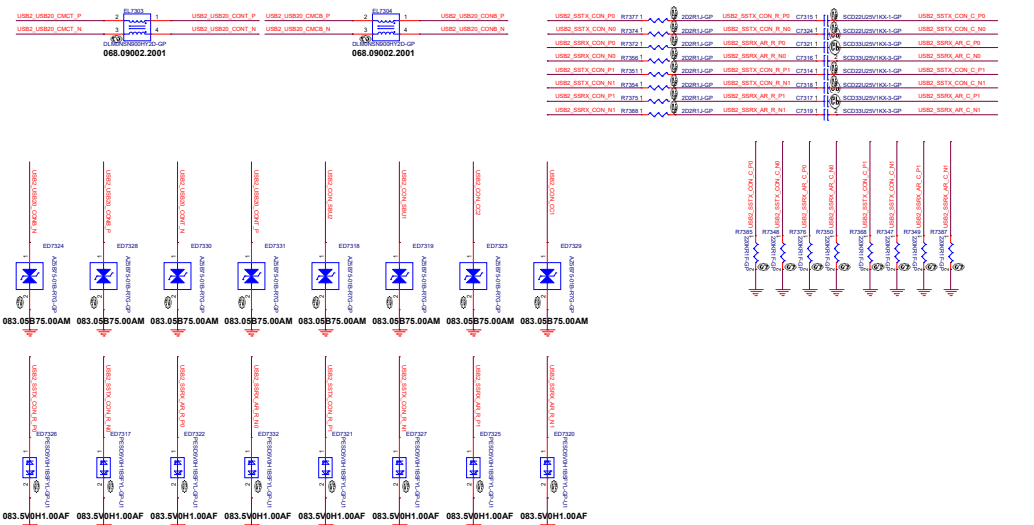
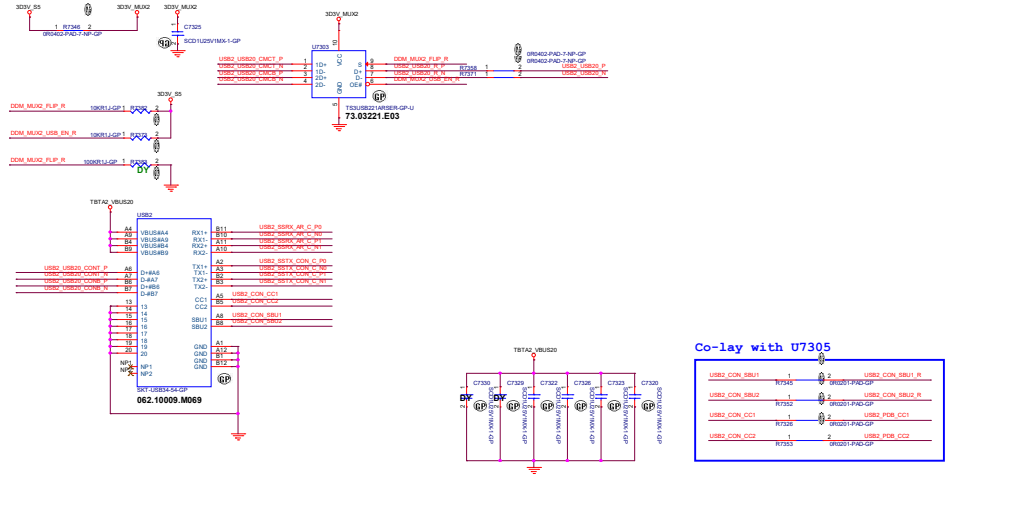
Main Func = TypeC



Close U7201 (p. 72)

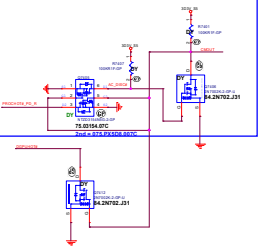


Main Func = Typ

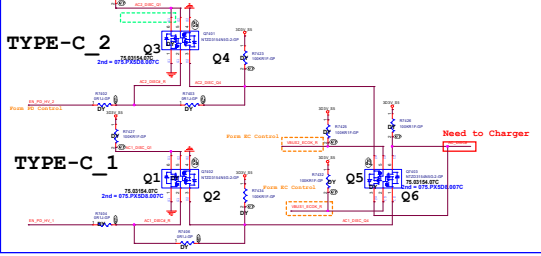


- 1. USB2.0_OTG_P2 >>>
- 2. USB2.0_OTG_P1 >>>
- 3. USB2.0_OTG_P3 >>>
- 4. USB2.0_OTG_P4 >>>
- 5. USB2.0_OTG_P5 >>>
- 6. USB2.0_OTG_P6 >>>
- 7. USB2.0_OTG_P7 >>>
- 8. USB2.0_OTG_P8 >>>
- 9. USB2.0_OTG_P9 >>>
- 10. USB2.0_OTG_P10 >>>
- 11. USB2.0_OTG_P11 >>>
- 12. USB2.0_OTG_P12 >>>
- 13. USB2.0_OTG_P13 >>>
- 14. USB2.0_OTG_P14 >>>
- 15. USB2.0_OTG_P15 >>>
- 16. USB2.0_OTG_P16 >>>
- 17. USB2.0_OTG_P17 >>>
- 18. USB2.0_OTG_P18 >>>
- 19. USB2.0_OTG_P19 >>>
- 20. USB2.0_OTG_P20 >>>
- 21. USB2.0_OTG_P21 >>>
- 22. USB2.0_OTG_P22 >>>
- 23. USB2.0_OTG_P23 >>>
- 24. USB2.0_OTG_P24 >>>
- 25. USB2.0_OTG_P25 >>>
- 26. USB2.0_OTG_P26 >>>
- 27. USB2.0_OTG_P27 >>>
- 28. USB2.0_OTG_P28 >>>
- 29. USB2.0_OTG_P29 >>>
- 30. USB2.0_OTG_P30 >>>
- 31. USB2.0_OTG_P31 >>>
- 32. USB2.0_OTG_P32 >>>
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- 64. USB2.0_OTG_P64 >>>
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- 90. USB2.0_OTG_P90 >>>
- 91. USB2.0_OTG_P91 >>>
- 92. USB2.0_OTG_P92 >>>
- 93. USB2.0_OTG_P93 >>>
- 94. USB2.0_OTG_P94 >>>
- 95. USB2.0_OTG_P95 >>>
- 96. USB2.0_OTG_P96 >>>
- 97. USB2.0_OTG_P97 >>>
- 98. USB2.0_OTG_P98 >>>
- 99. USB2.0_OTG_P99 >>>
- 100. USB2.0_OTG_P100 >>>

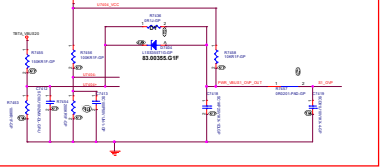
AC Disconnect Latch



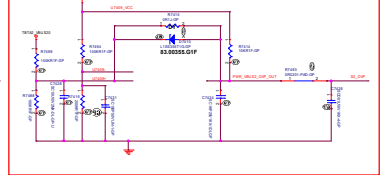
AC_Disconnect_Logics



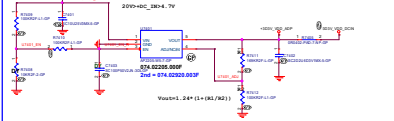
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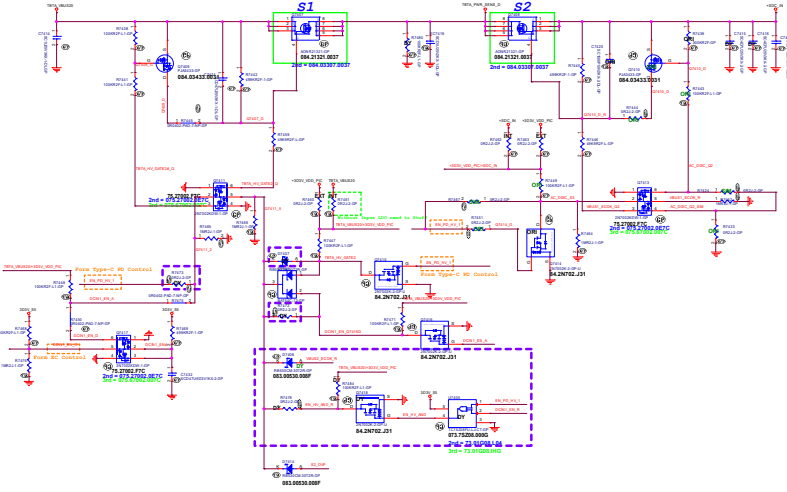
VBUS_OVP



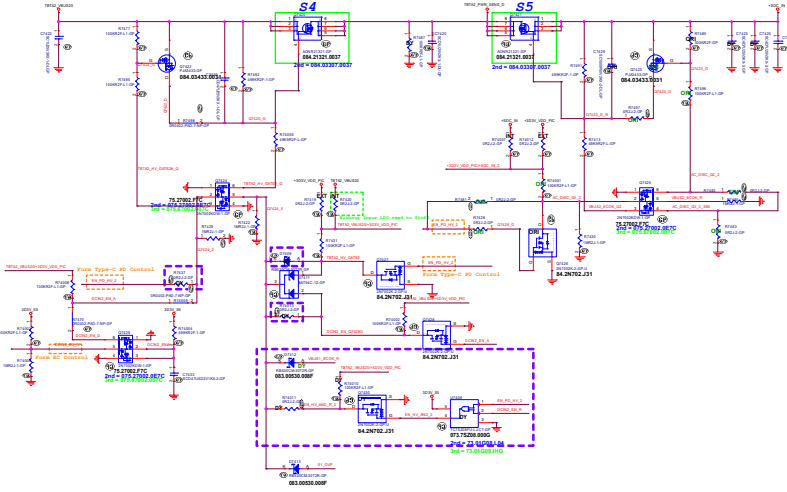
+3D3V_VDD_DCIN

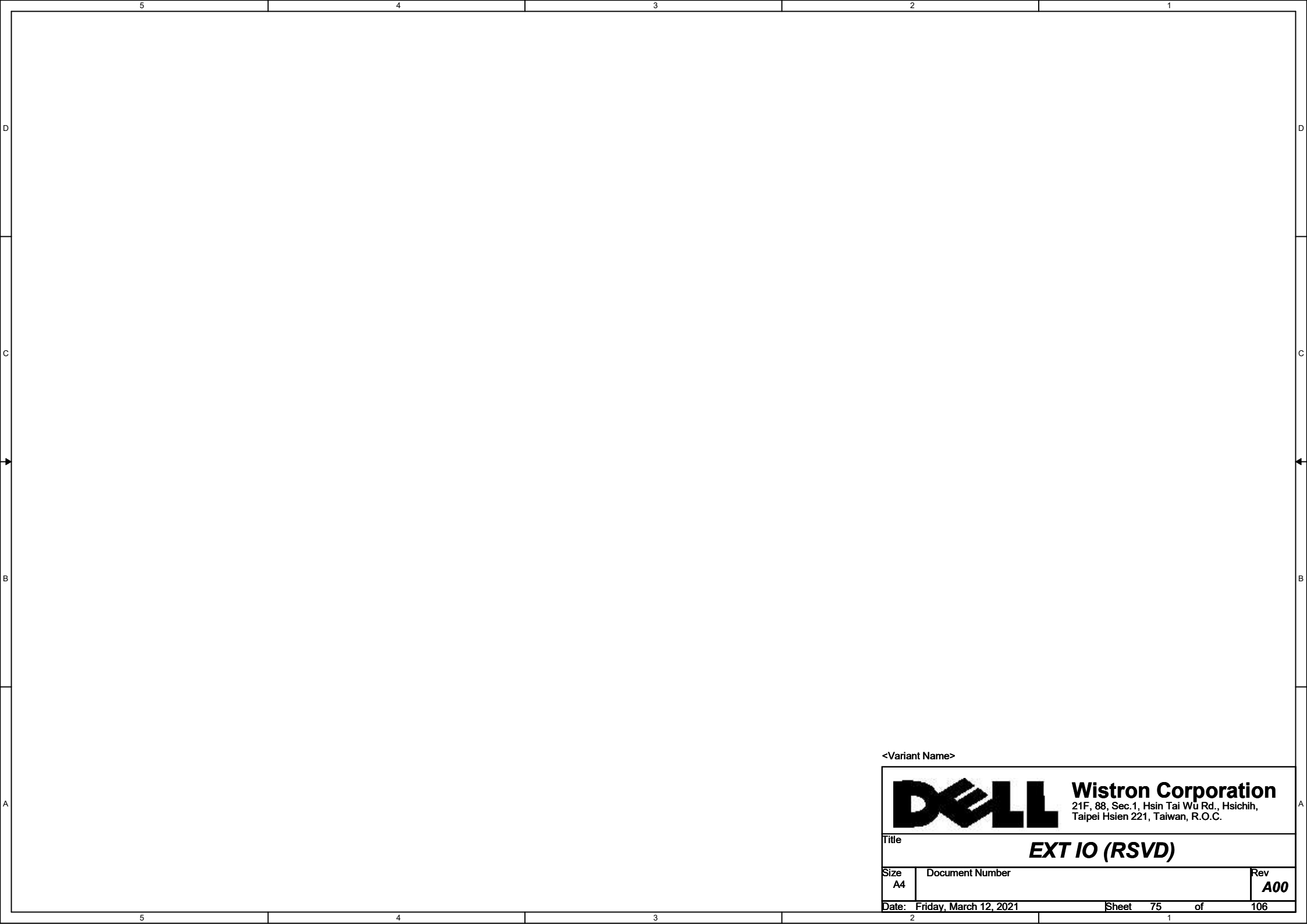


TYPE-C 1




TYPE-C 2



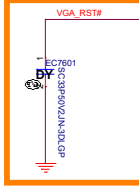


<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title EXT IO (RSVD)			
Size A4	Document Number		Rev A00
Date: Friday, March 12, 2021	Sheet 75 of		106

21 DGPU_HOLD_RST# >>>
21,24,85 DGPU_PWROK >>>
20 CLK_PCIE_PEG_REQ# >>>
79 VGA_RST# >>>
19 GFX_CLK_CPU_P >>>
19 GFX_CLK_CPU_N >>>

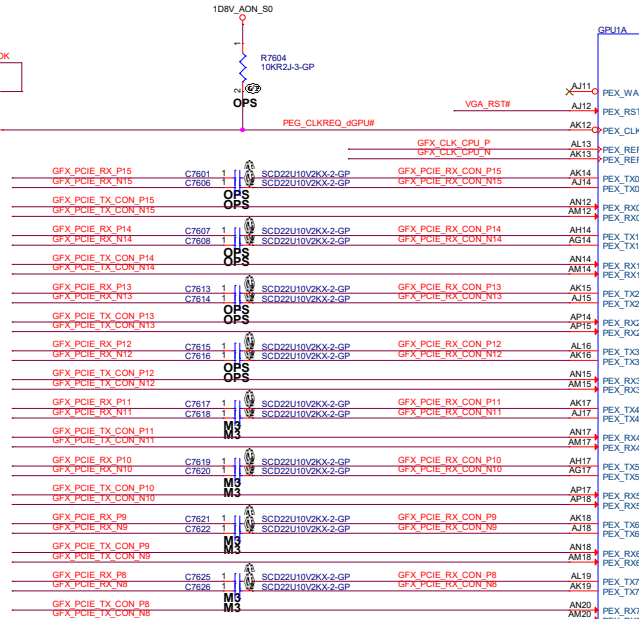
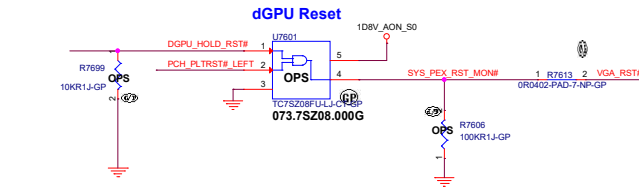
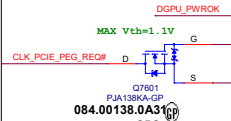
EMI Reserved



3 GFX_PCIE_RX_P15
3 GFX_PCIE_RX_N15
3 GFX_PCIE_RX_P14
3 GFX_PCIE_RX_N14
3 GFX_PCIE_RX_P13
3 GFX_PCIE_RX_N13
3 GFX_PCIE_TX_CON_P12
3 GFX_PCIE_TX_CON_N12
3 GFX_PCIE_TX_CON_P11
3 GFX_PCIE_TX_CON_N11
3 GFX_PCIE_TX_CON_P10
3 GFX_PCIE_TX_CON_N10
3 GFX_PCIE_TX_CON_P9
3 GFX_PCIE_TX_CON_N9
3 GFX_PCIE_TX_CON_P8
3 GFX_PCIE_TX_CON_N8

3 GFX_PCIE_TX_CON_P15
3 GFX_PCIE_TX_CON_N15
3 GFX_PCIE_TX_CON_P14
3 GFX_PCIE_TX_CON_N14
3 GFX_PCIE_TX_CON_P13
3 GFX_PCIE_TX_CON_N13
3 GFX_PCIE_TX_CON_P12
3 GFX_PCIE_TX_CON_N12
3 GFX_PCIE_TX_CON_P11
3 GFX_PCIE_TX_CON_N11
3 GFX_PCIE_TX_CON_P10
3 GFX_PCIE_TX_CON_N10
3 GFX_PCIE_TX_CON_P9
3 GFX_PCIE_TX_CON_N9
3 GFX_PCIE_TX_CON_P8
3 GFX_PCIE_TX_CON_N8

20,63,71,99 PCH_PLTRST#_LEFT >>>



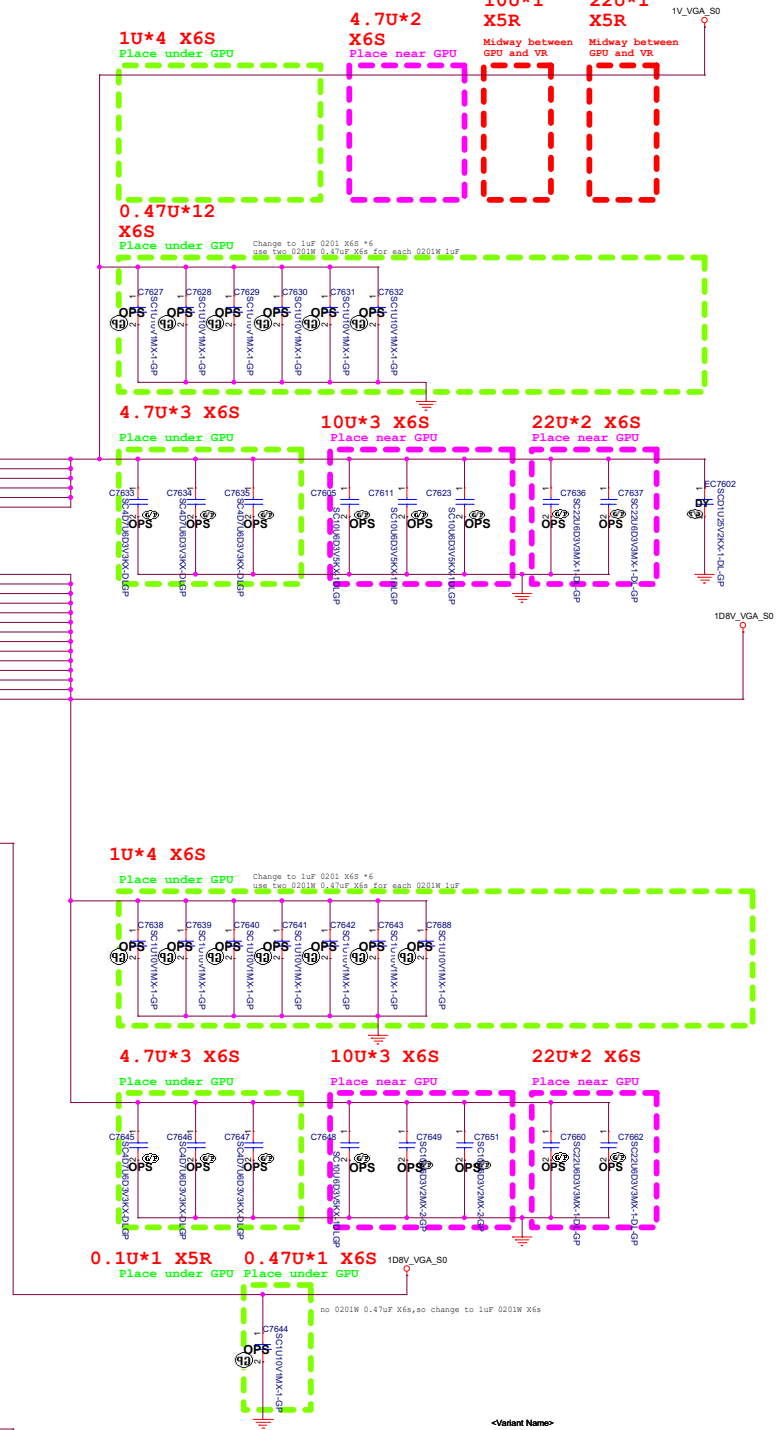
• PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
PEX_DVDD Supply Rail						
GB4C-128, GB4D-128	1.0 μ F	X65 0402 or 0201W	0	1	2	Under GPU
	0.47 μ F	X65 0201W	12	0	2	Under GPU
	4.7 μ F	X65 0603	0	2	2	Near GPU
	4.7 μ F	X65 0603	3	0	2	Under GPU
	10 μ F	X5R 0805	0	1	1	Midway between GPU and power supply
	10 μ F	X65 0805	3	0	2	Near GPU
	22 μ F	X5R 0805	0	1	1	Midway between GPU and power supply
	22 μ F	X65 0805	2	0	2	Near GPU

PEX_HVDD Supply Rail	Capacitor Type	Footprint	Population	N18	N17	Location
GB4C-128, GB4D-128	1.0 μ F	X65 0402 or 0201W	0	1	2	Under GPU
	0.47 μ F	X65 0201W	13	0	2	Under GPU
	4.7 μ F	X65 0603	0	2	2	Near GPU
	4.7 μ F	X65 0603	3	0	2	Under GPU
	10 μ F	X5R 0805	0	1	1	Midway between GPU and power supply
	10 μ F	X65 0805	3	0	2	Near GPU
	22 μ F	X5R 0805	0	1	1	Midway between GPU and power supply
	22 μ F	X65 0805	2	0	2	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

071.0N18P.0A00
OPS



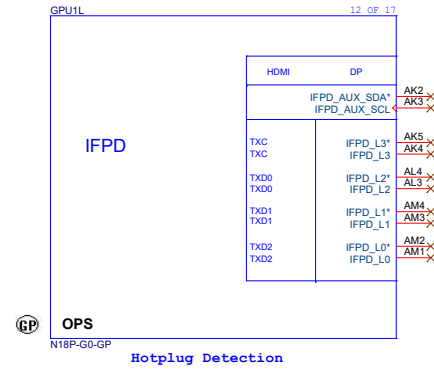
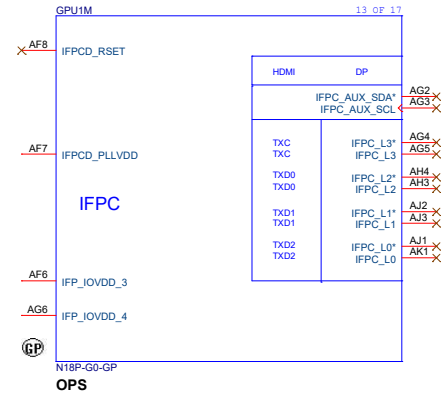
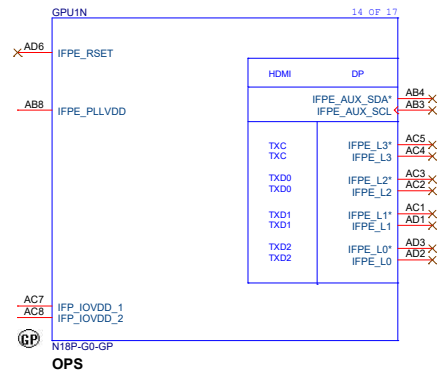
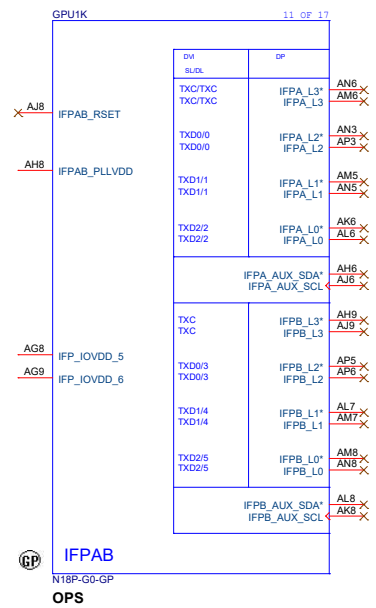


Table 7. IFPy_JOVDD Decoupling and Filtering

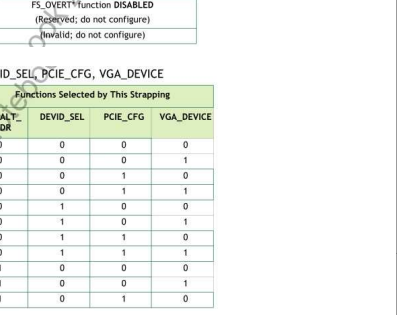
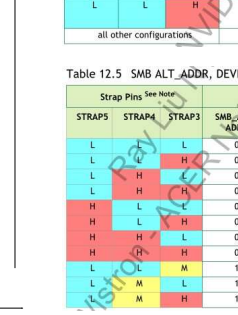
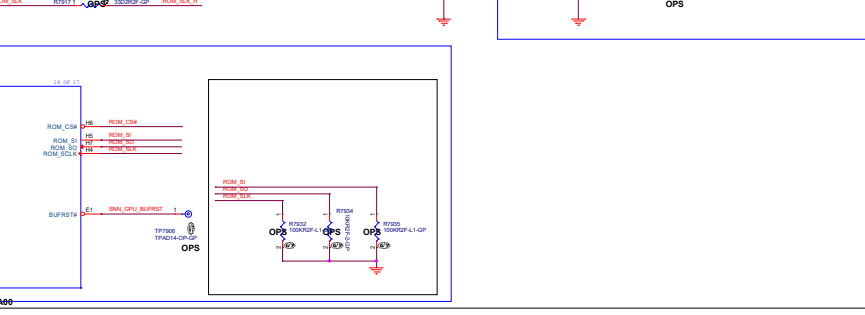
GPU	Type	Footprint	Population	N18	N17	Location
IFP_JOVDD Supply Rails						
GB4C-128, GB4D-128	0.1 μ F	X78	0402	0	6	Under GPU; 1 per ball
	0.47 μ F	X65	0201W	0	0	Under GPU; 1 per ball
	1.0 μ F	X65	0402 or 0201W	0	3	Near GPU
	0.47 μ F	X65	0201W	6	0	Near GPU
	4.7 μ F	X65	0603	3	3	Near GPU
Bead Type						
180 Ω @ 100 MHz (ESR<0.2 Ω)			0603	0	0	Near GPU

Note:
 1. Design may alternatively use one 0201W 0.47 μ F X65 for each 0201W 1 μ F.
 2. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

<Variant Name>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU (DIGITAL 2/5)			
Size	Document Number		Rev
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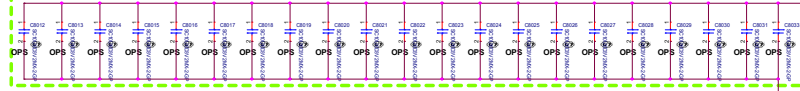
Strap Pins (see notes)			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMBALT_ADDR	DEV_IDSEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	H	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	L	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Strap Ping see Note			RAMC0 Getting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	M	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

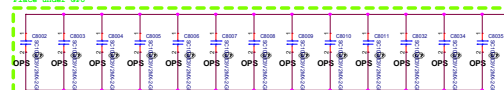
Memory Density	Allowed Memory Configuration	FBDVD/0	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14A	D-die	0x1	8 Gbps	1940		Full	Production candidate
			Samsung	K4Z803256BHC14	C-die	0x0	14 Gbps	2001		Full	Production candidate

Memory Density	Allowed Memory Configuration	FBVD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Cm256Mx16	1.2V	Micron	AT616 K2326M31E-14A	A-die	0x1	14 Gbps	1940*	Full	Production ready
			Samsung	K4Z803259C-HC14	C-die	0x0	14 Gbps	2001*	Full	Production ready
			Hynix	H56C8H24AIR-52C	A-die	0x2	14 Gbps	N/A	Full	Production ready

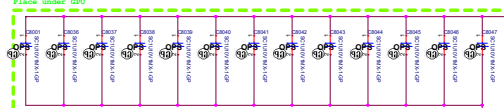
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100*13
Place under GPU



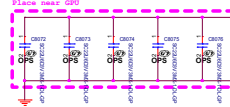
10*13
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0.47U*26
Place under GPU



22U*5
Place near GPU



22U*10
Place near GPU

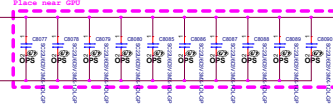


Table 2. NVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
NVDD Supply Net					
GB4C-128, GB4D-128	10 μ F	X65 0603	34	21	Under GPU
	1 μ F ¹	X65 0402 or 0201W	0	13	Under GPU
	0.47 μ F ¹	X65 0402 or 0201W	26	0	Under GPU
	10 μ F	X65 0603	0	31	Near GPU
	22 μ F	X65 0805	15	10	Near GPU
	4.7 μ F	X65 0603	0	2	Near GPU
	330 μ F	POS 7343	0	1	Near GPU

Note:

1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

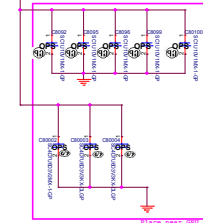
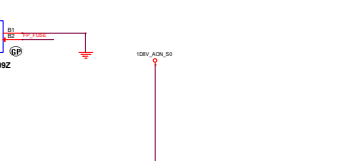
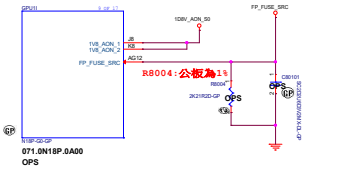
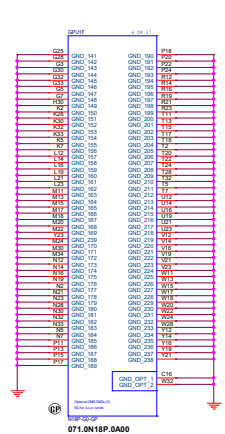
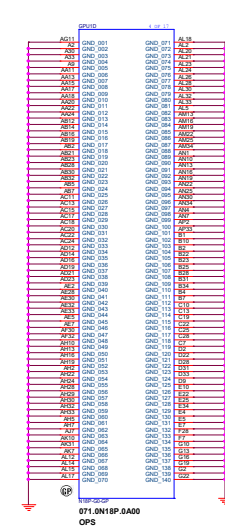
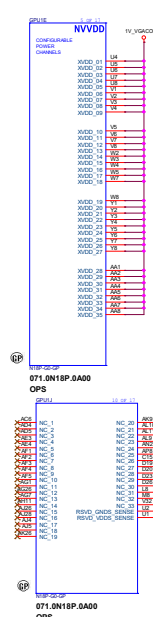
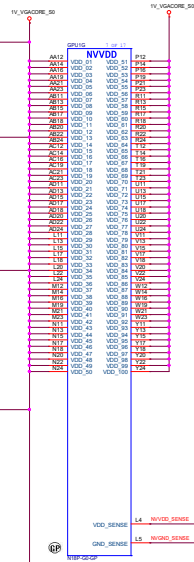
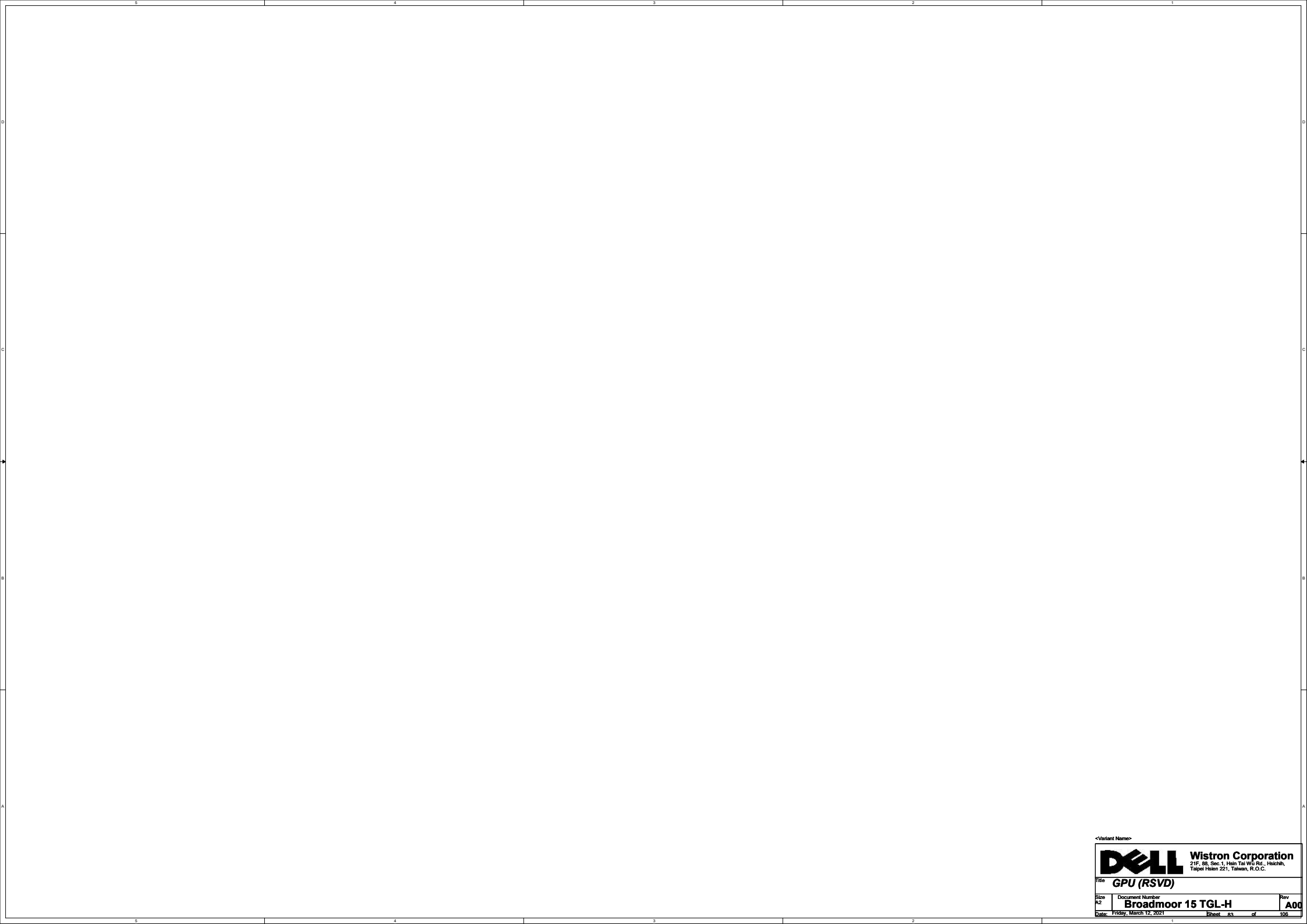


Table 9. VDD_AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
N17 VDD18 (N18 NC) Supply Rail					
GB4C-128, GB4D-128	0.1 μ F	X7R 0402	N/A	2	Under GPU
	1.0 μ F	X65 0603	N/A	1	Near GPU
	4.7 μ F	X65 0603	N/A	1	Near GPU
1V8_AON Supply Rail					
GB4C-128, GB4D-128	0.1 μ F	X7R 0402	0	2	Under GPU
	0.47 μ F ¹	X65 0201W	4	0	Under GPU
	1.0 μ F ¹	X65 0402 or 0201W	0	1	Near GPU
	0.47 μ F ¹	X65 0201W	6	0	Near GPU
	4.7 μ F	X65 0603	3	1	Near GPU

Note:

1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.



<Variant Name>

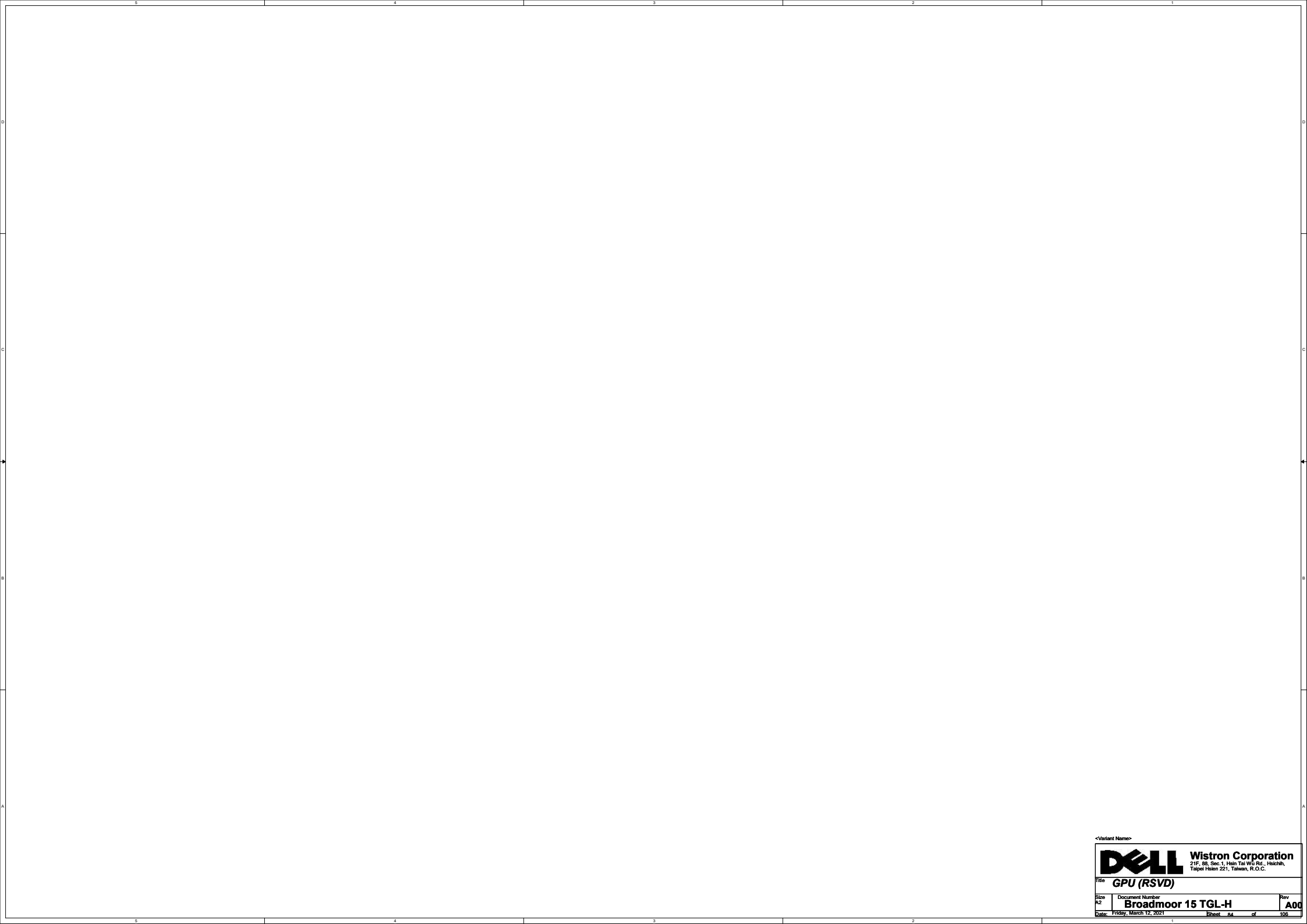


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Title	GPU (RSVD)		
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Size	Document Number	Rev
A2	Broadmoor 15 TGL-H	A00

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<Variant Name>

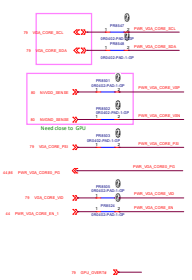


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Title **GPU (RSVD)**

Size A2 Document Number **Broadmoor 15 TGL-H** Rev **A00**

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For VGA_CORE sequence
EE need Check

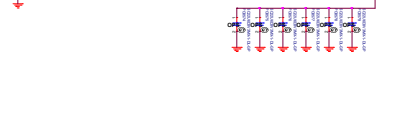
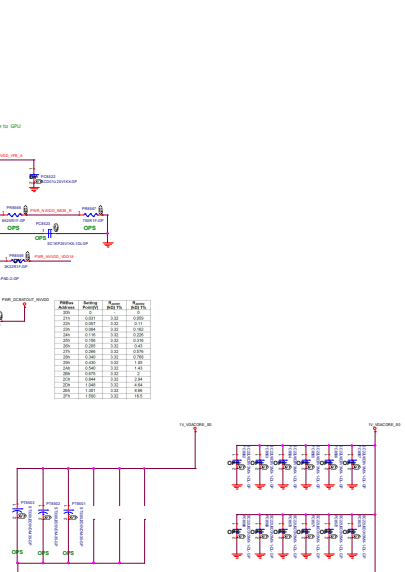
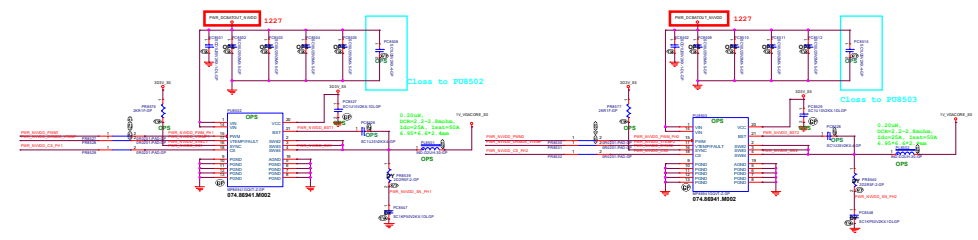
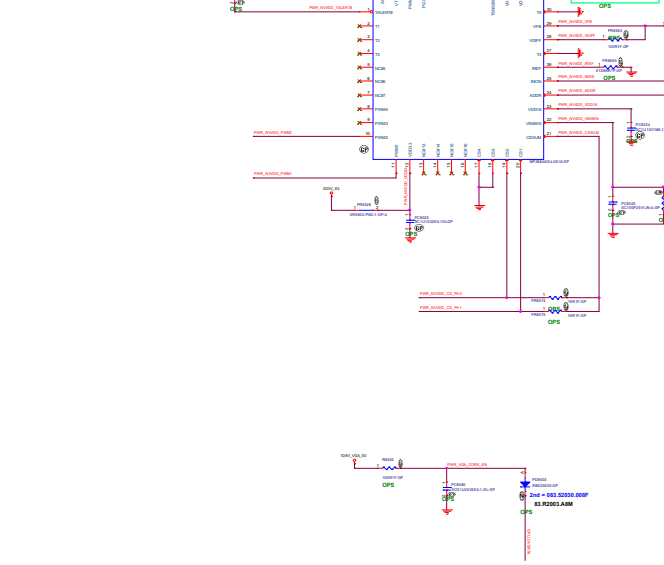
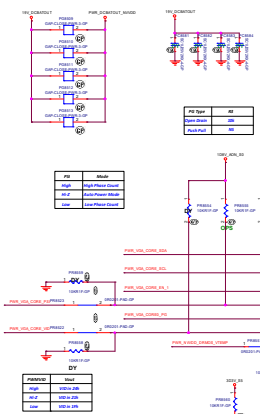
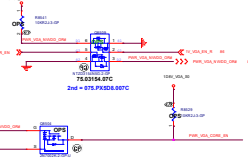


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F _{sw}	MHz	0.75
PWM Minimum Pulse Width T _{min}	ns	5.00
VID Transient Time T	us	<100
Component Value		
R1 (Ω)	KΩ	6.10
R2 (Ω)	KΩ	20.5
R3 (Ω)	KΩ	4.52
R4 (Ω)	KΩ	15.5
R5 (Ω)	KΩ	0.00
C	μF	0.3

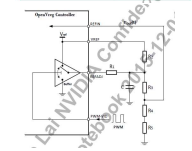
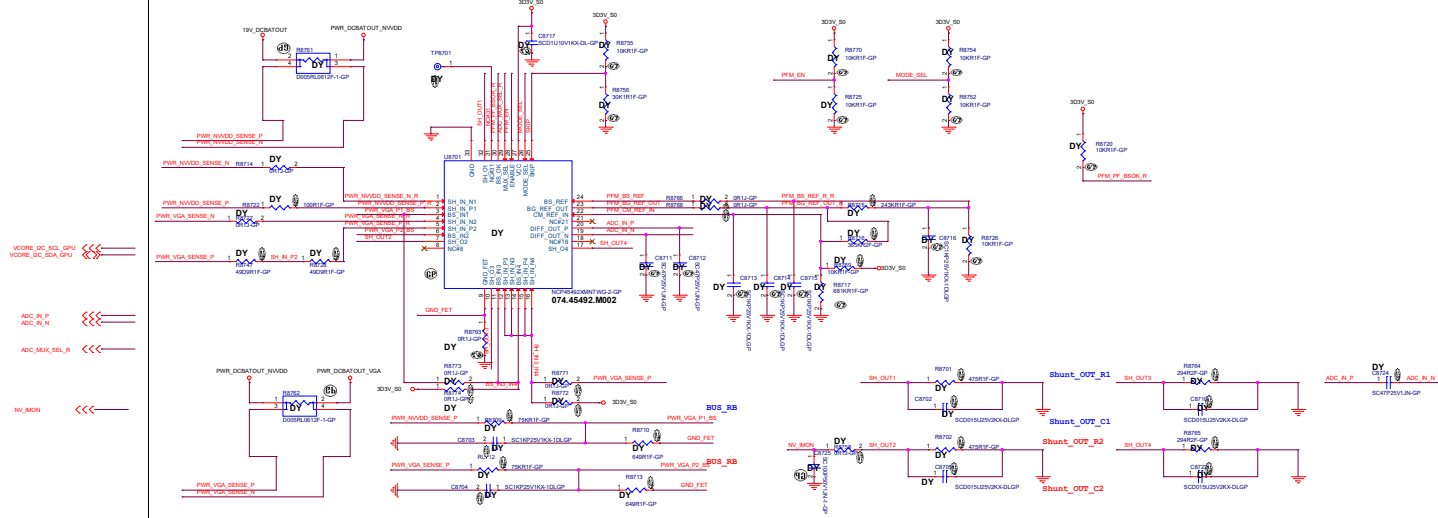


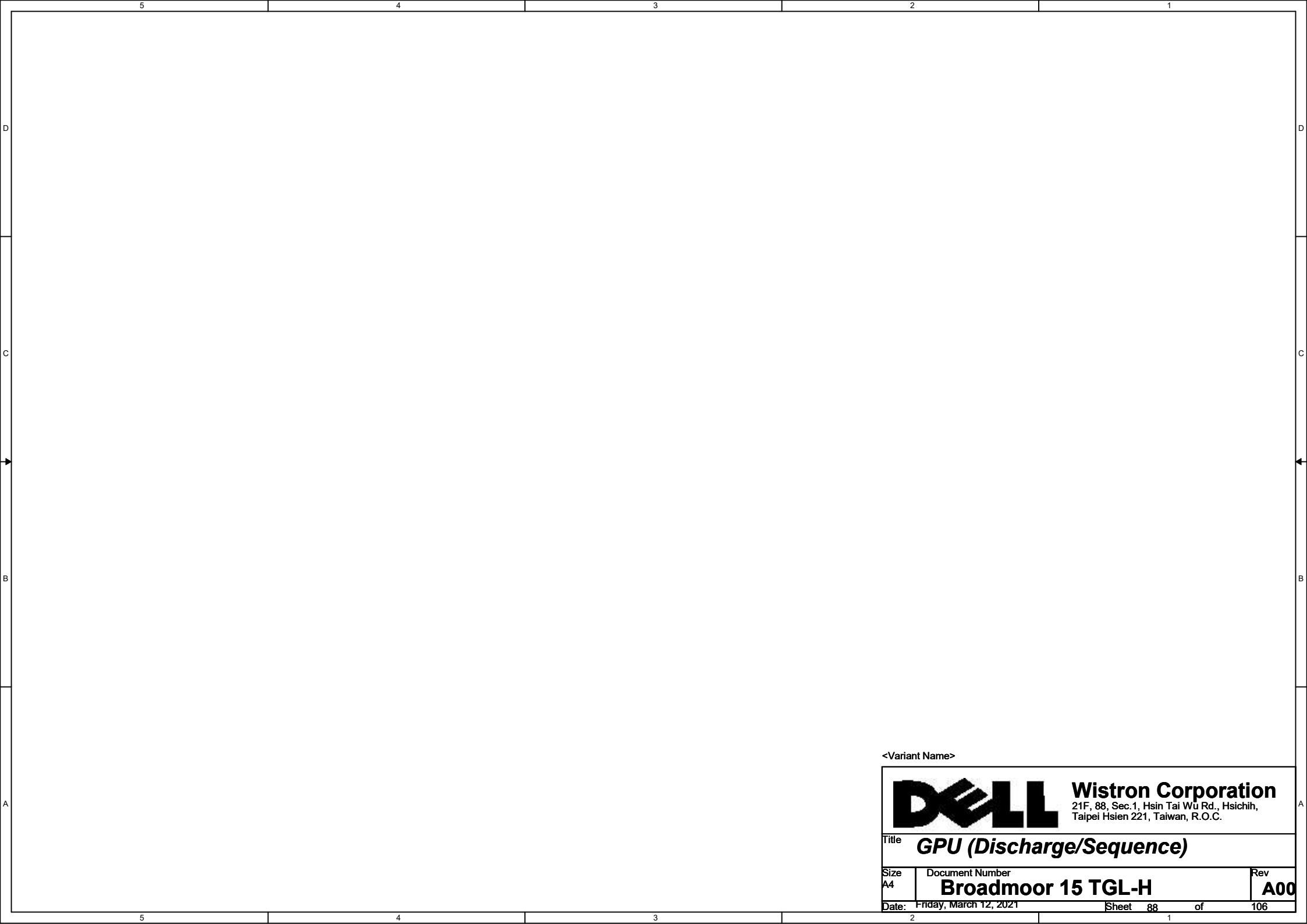
Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
V _{min}	V	0.3
V _{max}	V	1.3
V _{load}	V	0.8
Voltage Step V _{step}	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F _{sw}	MHz	0.75
PWM Minimum Pulse Width T _{min}	ns	5.00
VID Transient Time T	us	<100
Component Value		
R1 (Ω)	KΩ	6.10
R2 (Ω)	KΩ	20.5
R3 (Ω)	KΩ	4.52
R4 (Ω)	KΩ	15.5
R5 (Ω)	KΩ	0.00
C	μF	0.3




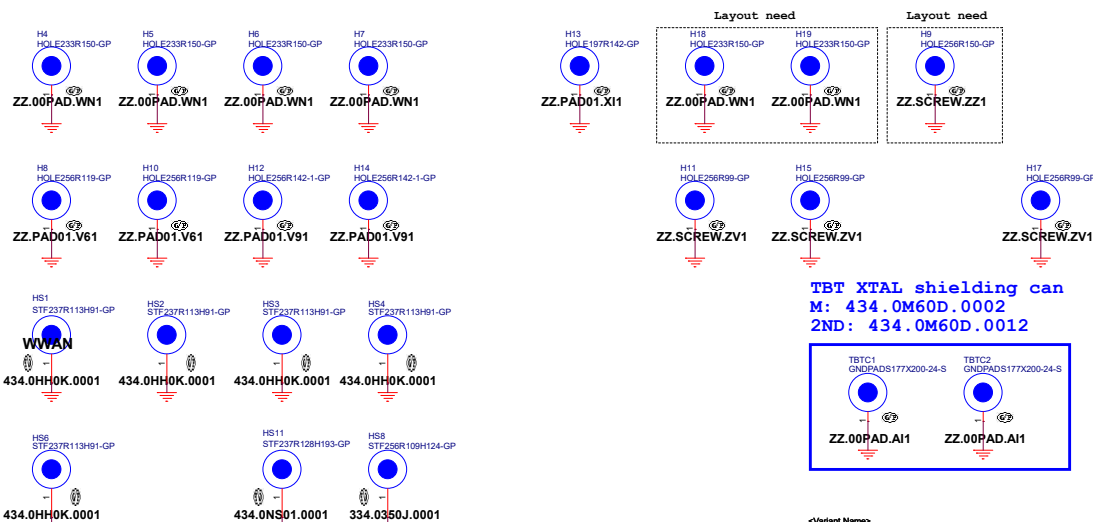
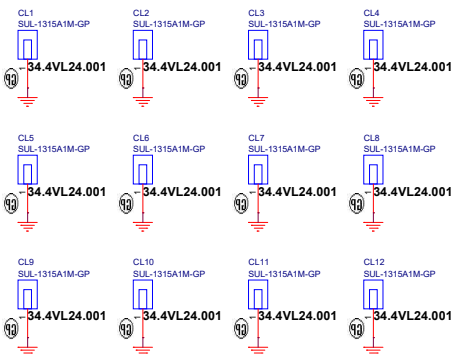
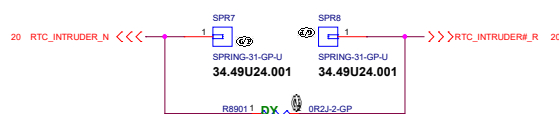
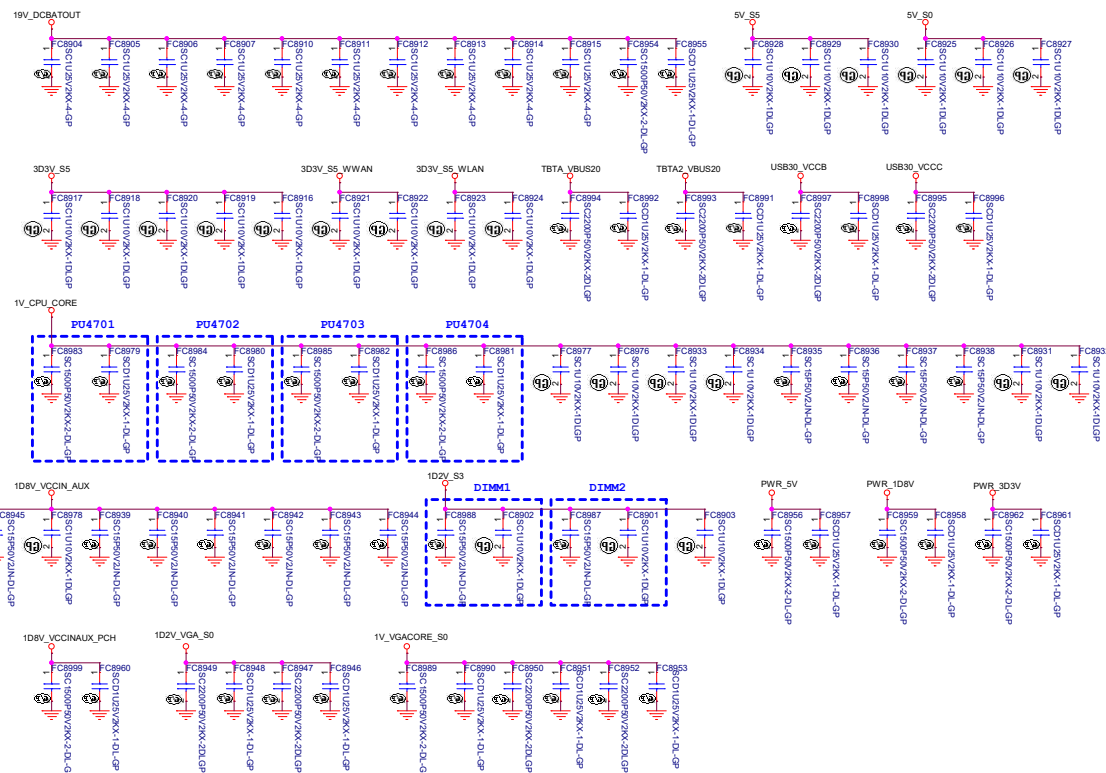
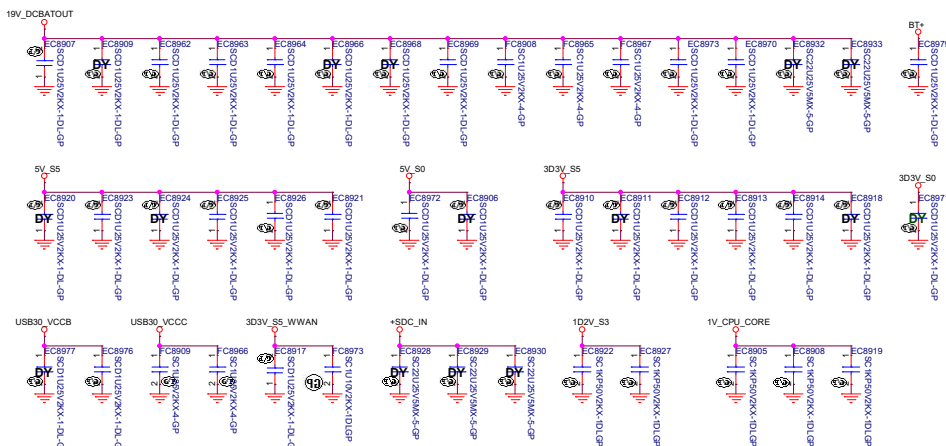
discharge circuit on page 86

Vcore_OVP circuit on page 44

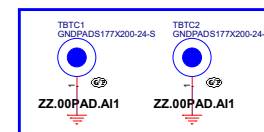


<Variant Name>

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Title GPU (Discharge/Sequence)					
Size A4		Document Number Broadmoor 15 TGL-H			Rev A00
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$$\text{Main Func} = \text{EMC} / \text{RF}$$


TBT XTAL shielding can
M: 434.0M60D.0002
2ND: 434.0M60D.0012



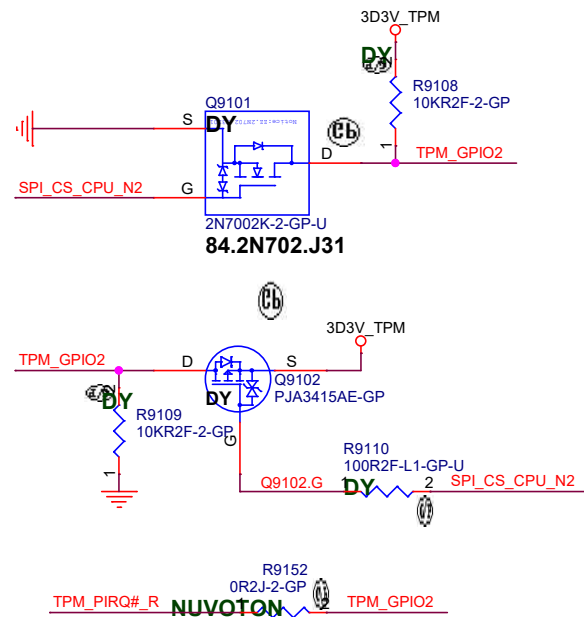
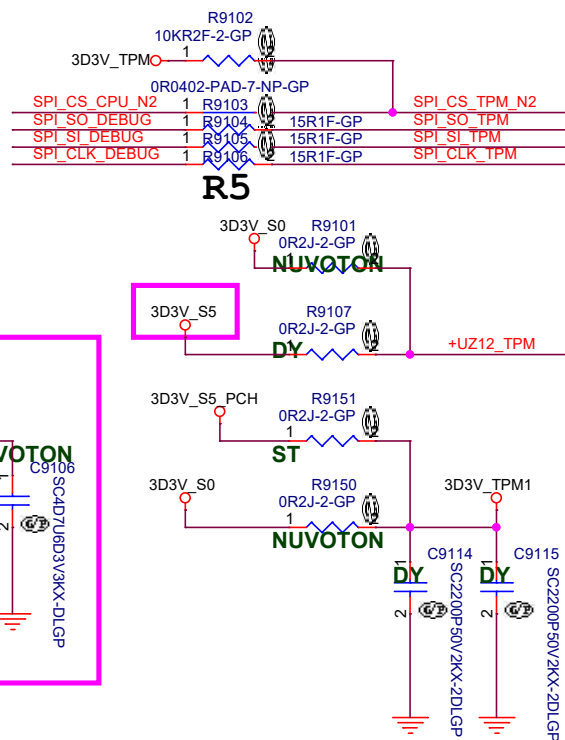
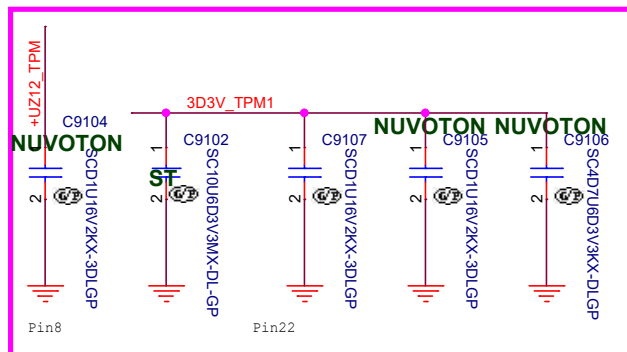
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C				C
B				B
A				A

<Variant Name>

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Title INT IO (RSVD) (NFC)		
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Main Func = TPM

20	TPM_PIRQ#
20,68	SIO_SLP_S0#
20,33,61,62,97	PCH_PLTRST#_RIGHT
24,25,68	SPI_CLK_DEBUG
24,25,68	SPI_SI_DEBUG
24,25,68	SPI_SO_DEBUG
18,96	SPI_CS_CPU_N2
21,40	CPU_C10_GATE#

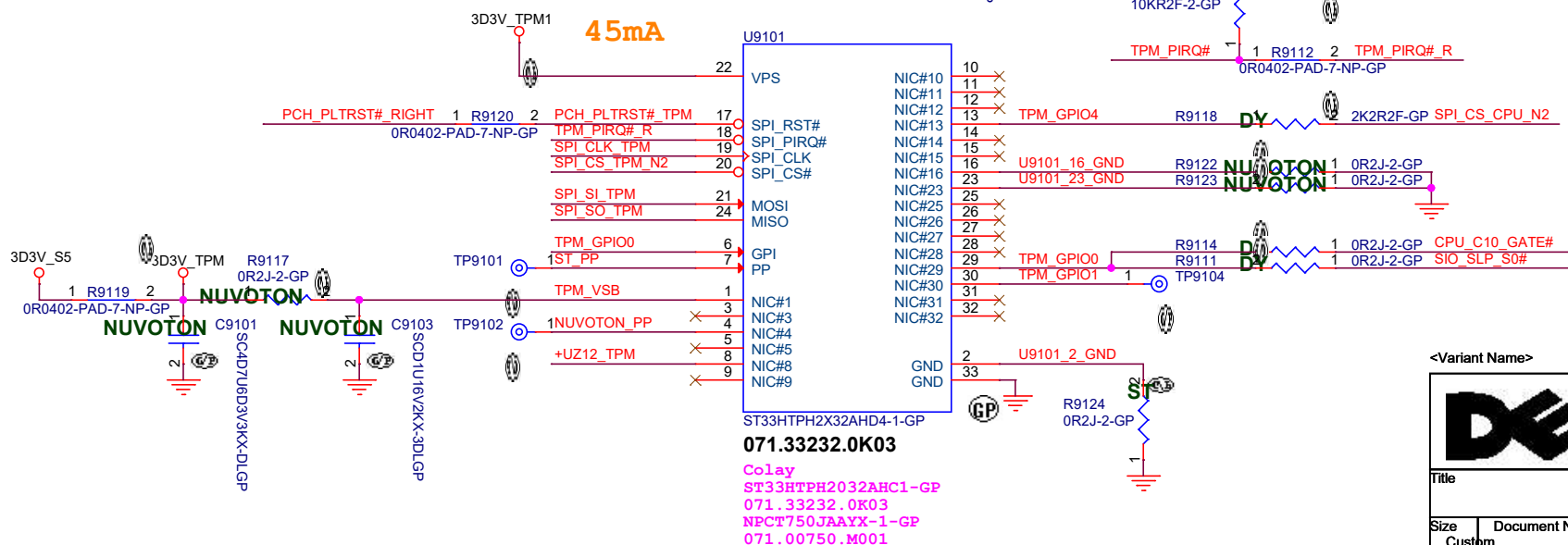
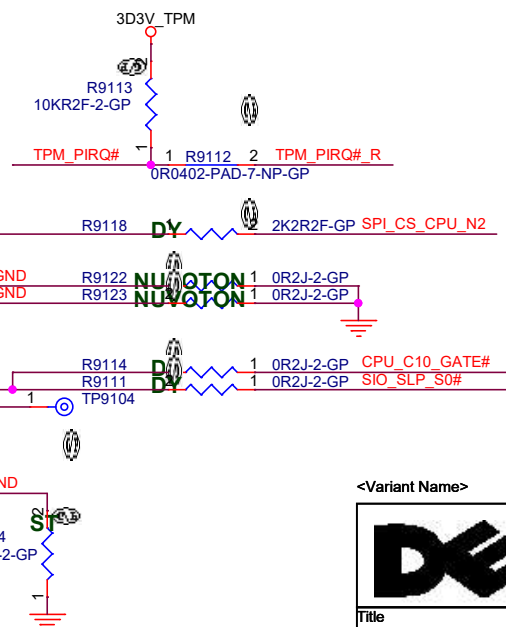


Close U9101 (p.91)

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96  SPI_CLK_TPM
96  SPI_SI_TPM
96  SPI_CS_TPM N2

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<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (TPM)

Size

Document Number

Custom

Rev

400

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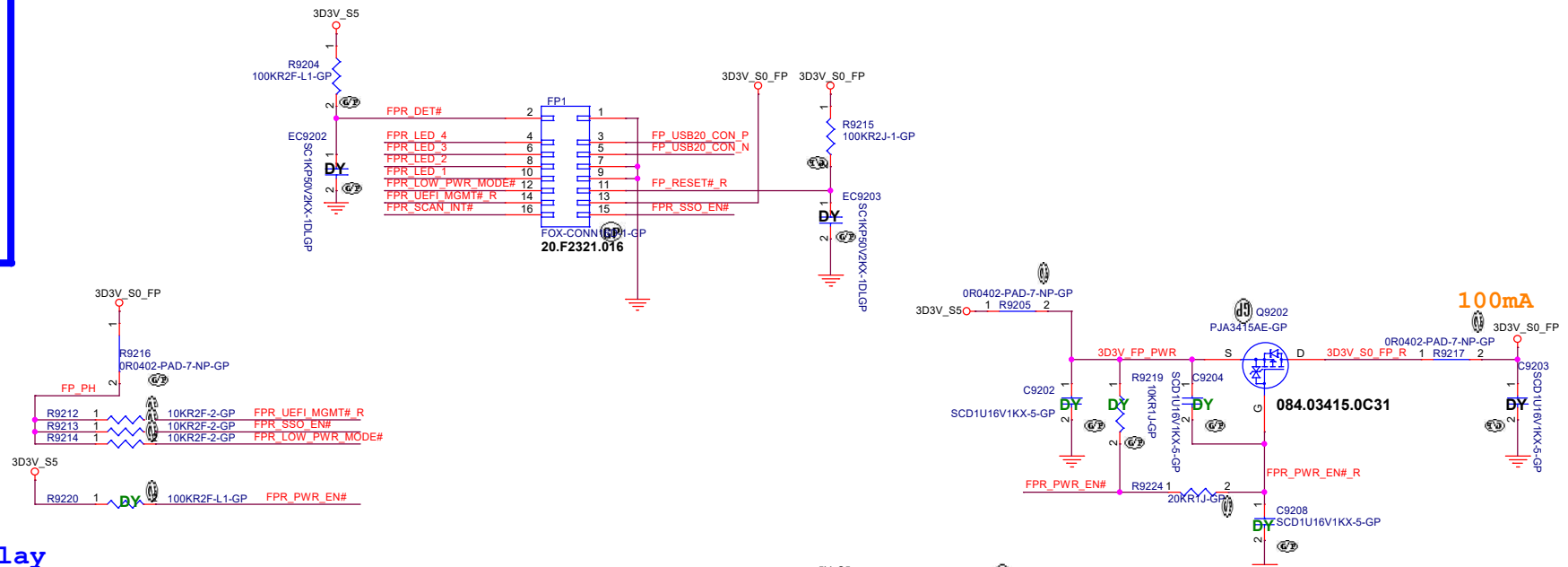
Date: Friday, March 12, 2021	
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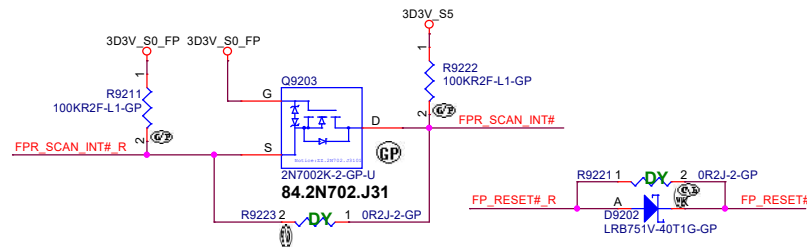
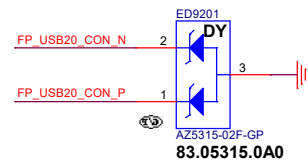
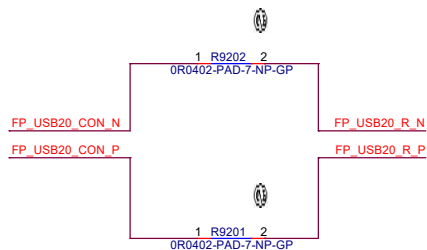
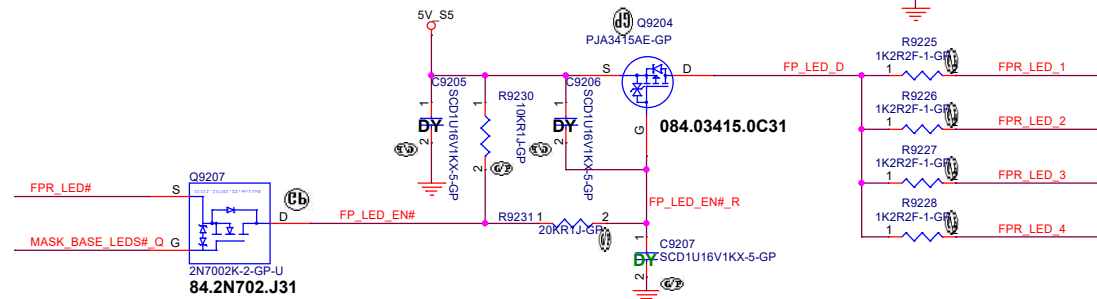
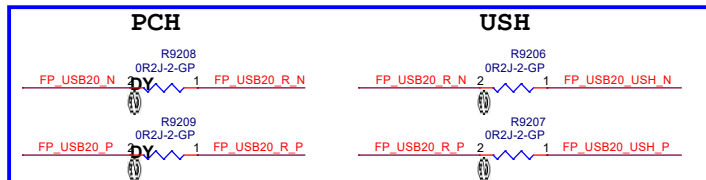
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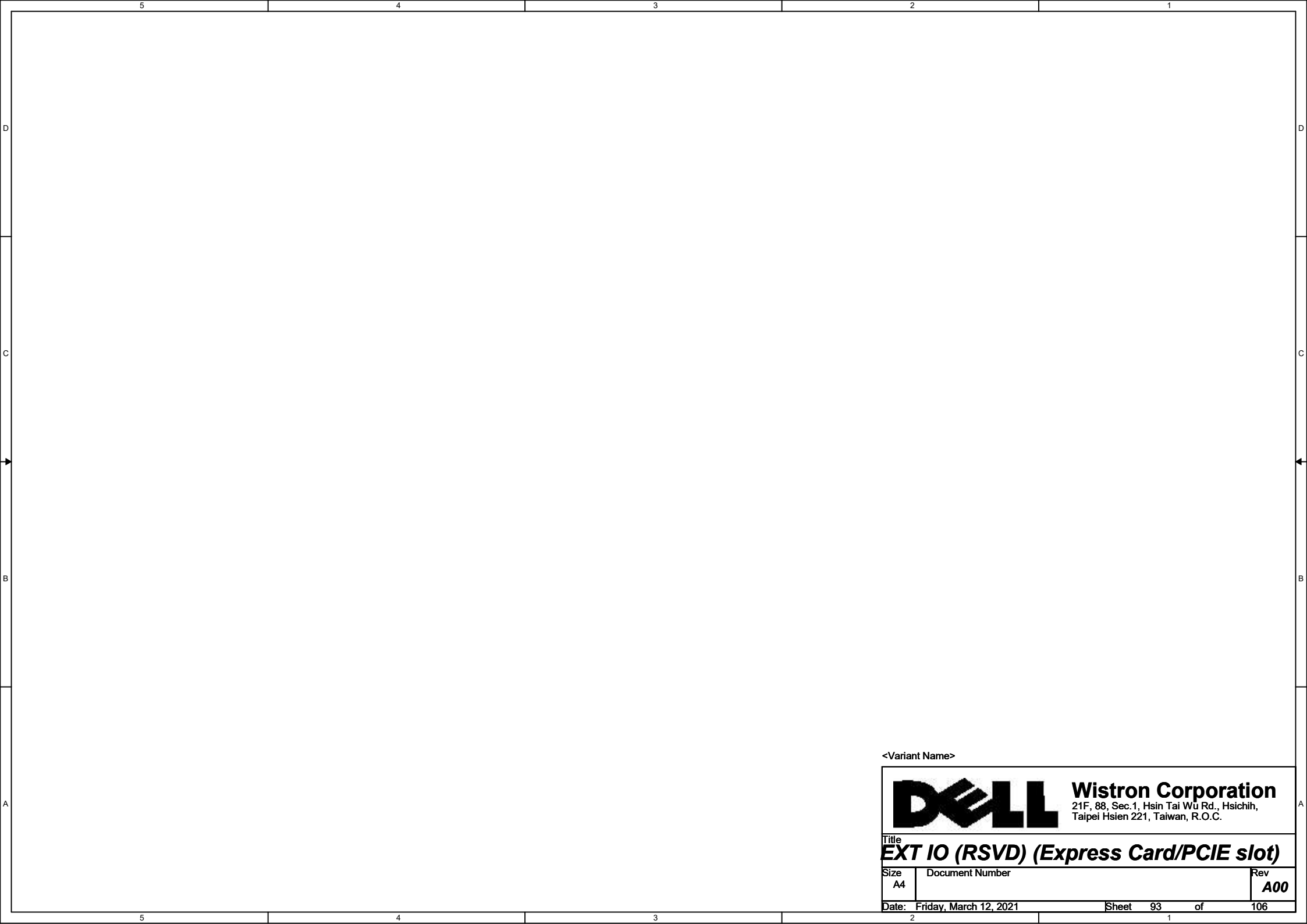
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66	FP_USB20_USH_P	<<<>>>
24	FPR_PWR_EN#	>>>>
24,66	FPR_SCAN_INT#	<<<<
24	FPR_SSO_EN#	>>>>
24	FPR_UEFI_MGMT#_R	>>>>
24	FPR_LOW_PWR_MODE#	>>>>
66	FP_RESET#	>>>>
24	FPR_LED#	<<<<
64	MASK_BASE_LEDS#_Q	>>>>




Try to co-lay






<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Express Card/PCIE slot)		
Size A4	Document Number	Rev A00
Date: Friday, March 12, 2021		Sheet 93 of 106


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C				C
B				B
A				A

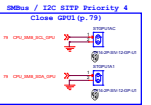
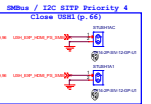
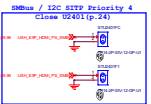
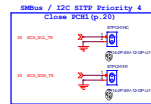
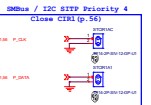
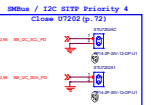
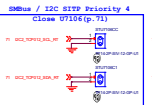
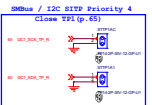
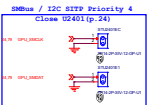
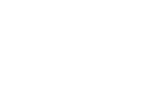
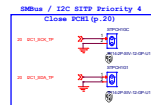
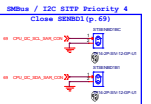
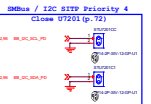
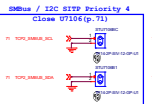
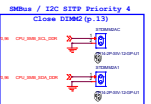
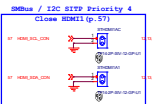
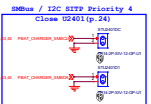
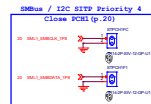
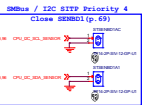
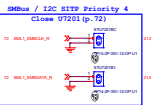
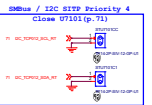
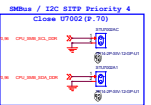
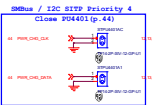
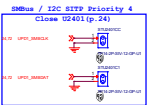
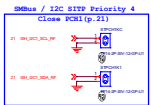
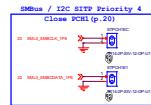
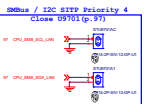
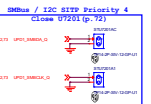
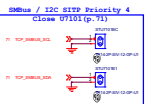
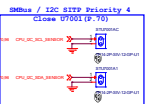
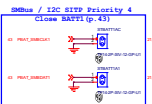
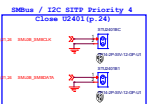
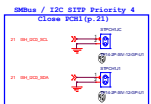
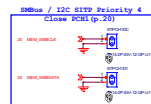
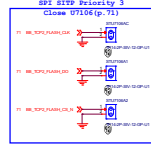
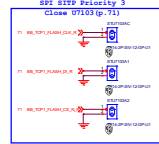
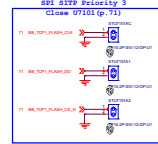
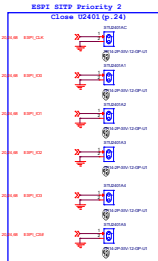
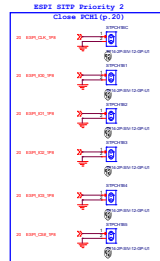
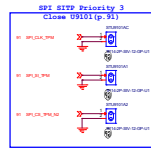
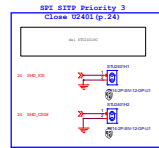
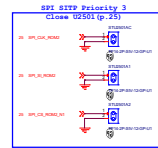
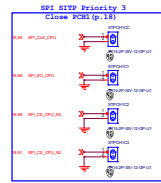
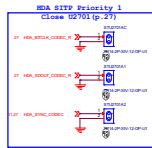
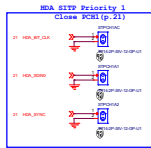
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Title EXT IO (RSVD) (Smart Card/COM/PS2)		
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5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Docking/LPT)		
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17 LAN_PCIE_RX_N
17 LAN_PCIE_RX_P
17 LAN_PCIE_TX_N
17 LAN_PCIE_TX_P

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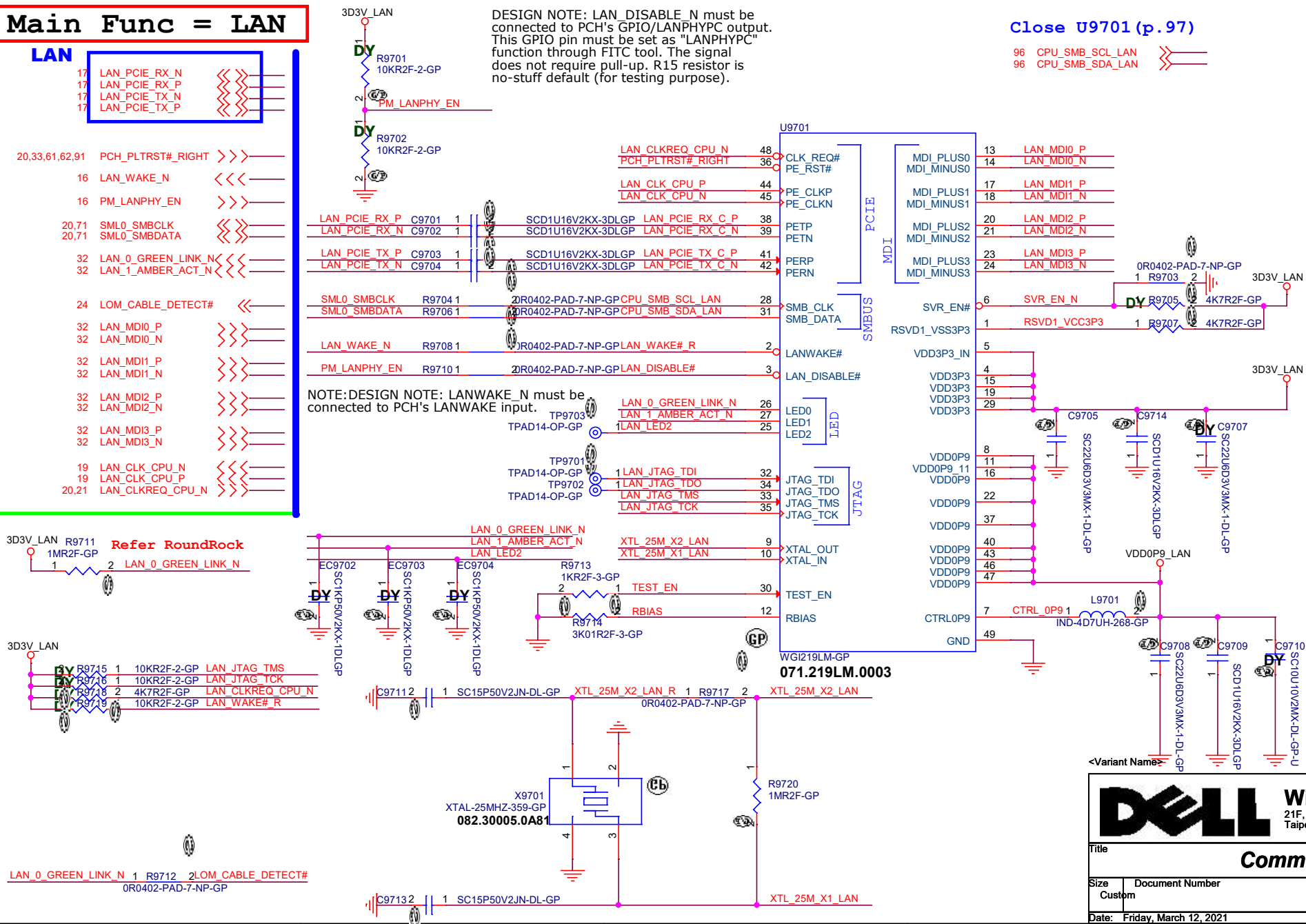
20,33,61,62,91	PCH_PLTRST#_RIGHT	>>>	_____
16	LAN_WAKE_N	<<<	_____
16	PM_LANPHY_EN	>>>	_____
20,71	SML0_SMBCLK	<<<	_____
20,71	SML0_SMBDATA	>>>	_____
32	LAN_0_GREEN_LINK_N	<<<	_____
32	LAN_1_AMBER_ACT_N	<<<	_____
24	LOM_CABLE_DETECT#	<<<	_____
32	LAN_MDIO_P	>>>	_____
32	LAN_MDIO_N	>>>	_____
32	LAN_MD10_P	>>>	_____
32	LAN_MD11_N	>>>	_____
32	LAN_MD12_P	>>>	_____
32	LAN_MD12_N	>>>	_____
32	LAN_MD13_P	>>>	_____
32	LAN_MD13_N	>>>	_____
19	LAN_CLK_CPU_N	<<<	_____
19	LAN_CLK_CPU_P	<<<	_____
20,21	LAN_CLKREQ_CPU_N	>>>	_____

Close U9701 (p.97)

```

96 CPU_SMB_SCL_LAN
96 CPU_SMB_SDA_LAN

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Wistron Corporation

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Title	Commercial (Intel LAN)
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Size	Document Number	Rev
Custom		400

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5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Commercial (LAN Switch)		
Size A4	Document Number	Rev A00
Date: Friday, March 12, 2021		Sheet 98 of 106

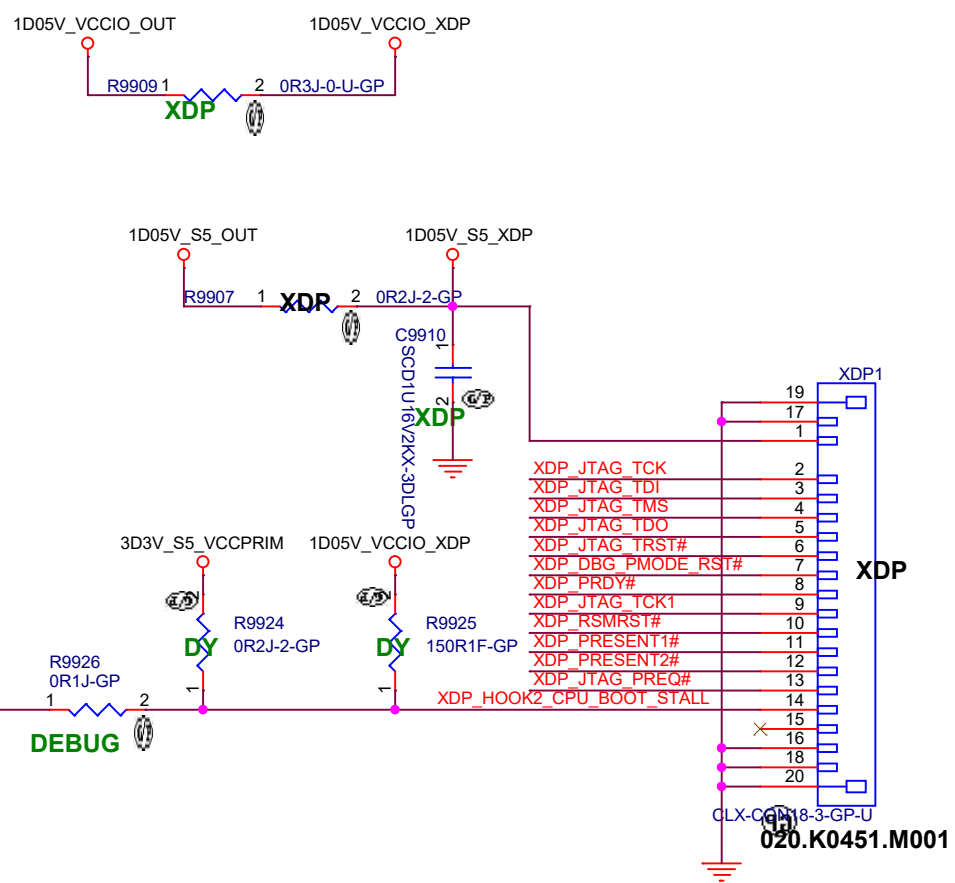
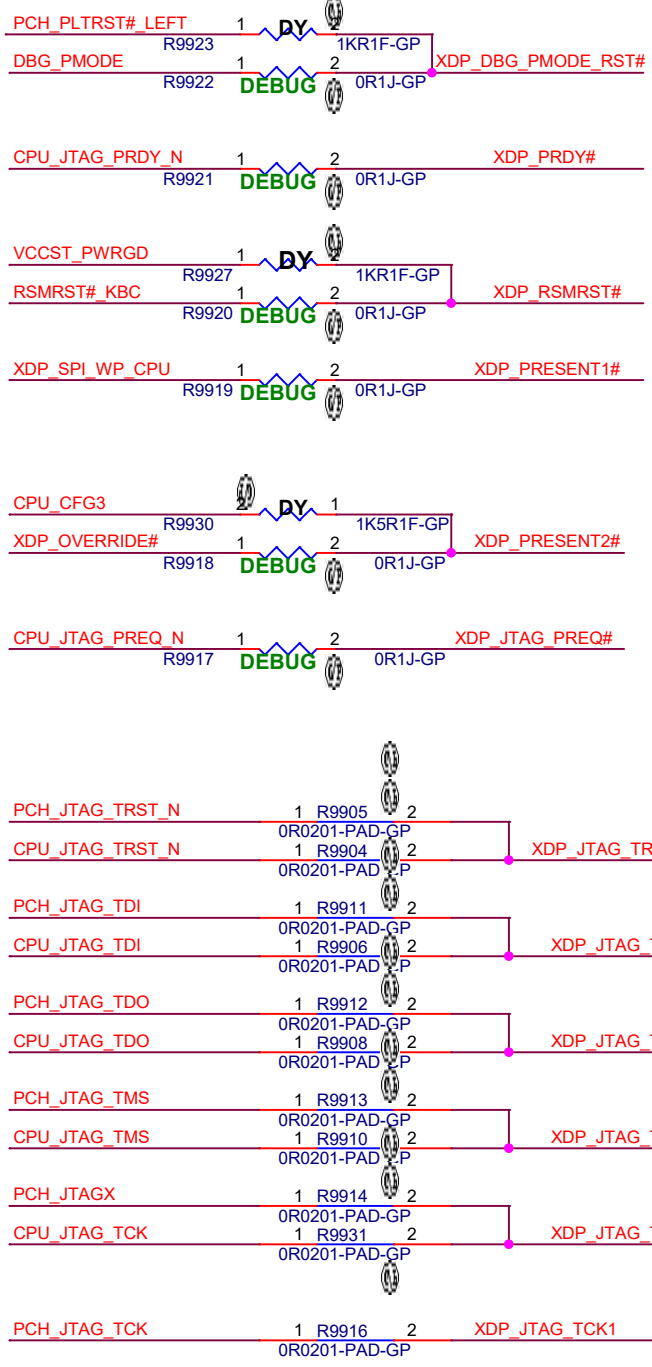
Main Func = Debug

6 CPU_CFG3 <<<—

6 VCCST_PWRGD <<<—
4,99 CPU_EAR <<<—
20,63,71,76 PCH_PLTRST#_LEFT <<<—
11,20 DBG_PMODE <<<—
6,17 CPU_JTAG_PRDY_N <<<—
16,17,24,64 RSMRST#_KBC <<<—
68 XDP_SPI_WP_CPU <<<—
40 XDP_OVERRIDE# <<<—
6,17 CPU_JTAG_PREQ_N <<<—
4,99 CPU_EAR <<<—

20 PCH_JTAG_TCK <<>>—
6 CPU_JTAG_TRST_N <<>>—
6 CPU_JTAG_TCK <<>>—
6 CPU_JTAG_TDI <<>>—
6 CPU_JTAG_TDO <<>>—
6 CPU_JTAG_TMS <<>>—

19 PCH_JTAG_TRST_N <<>>—
20 PCH_JTAGX <<>>—
20 PCH_JTAG_TMS <<>>—
20 PCH_JTAG_TDO <<>>—
20 PCH_JTAG_TDI <<>>—



<Variant Name>


			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Debug (XDP debug)					
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603


The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>



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Title

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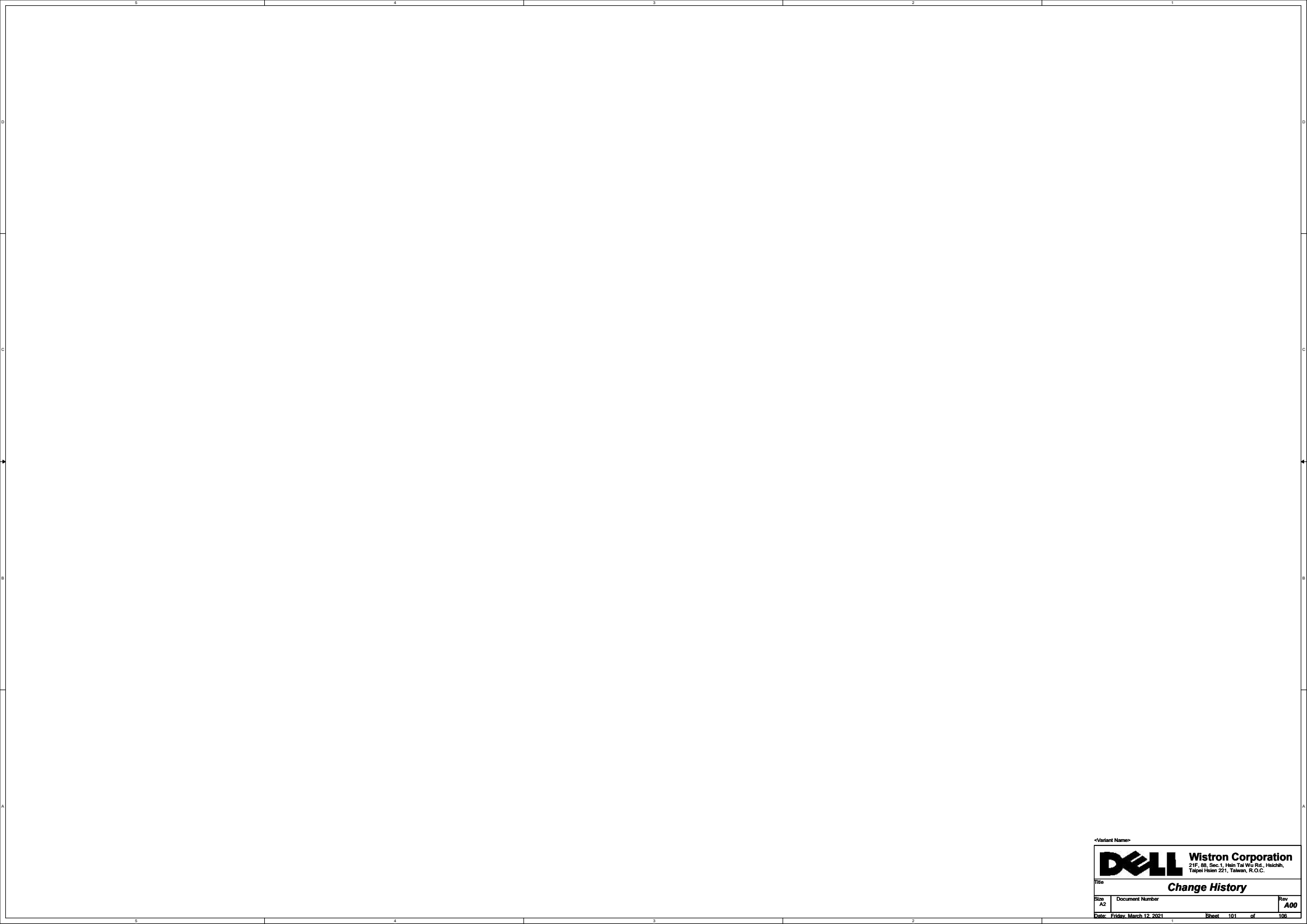
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Document Number


Rev
A00

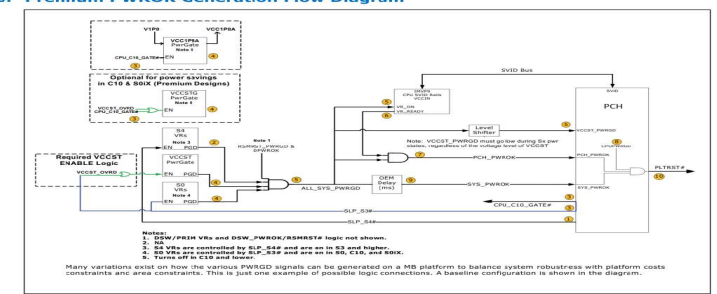
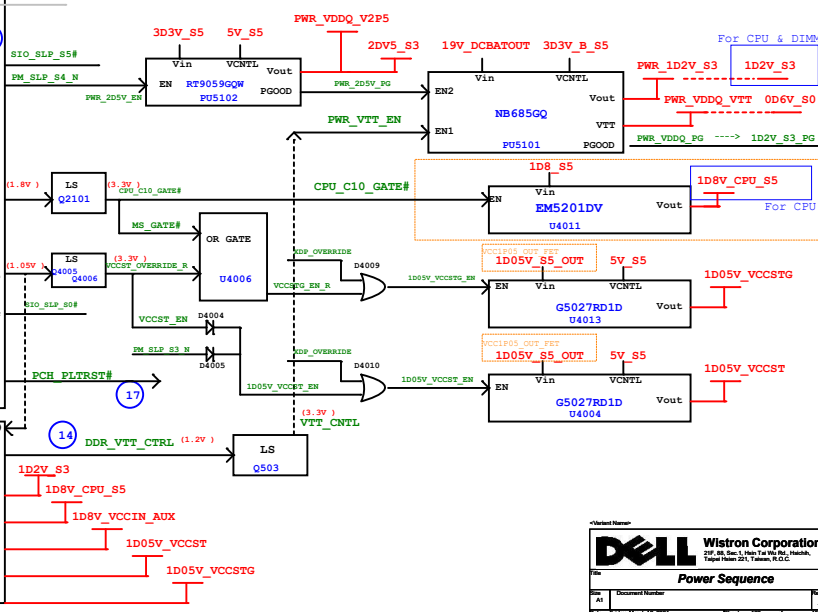
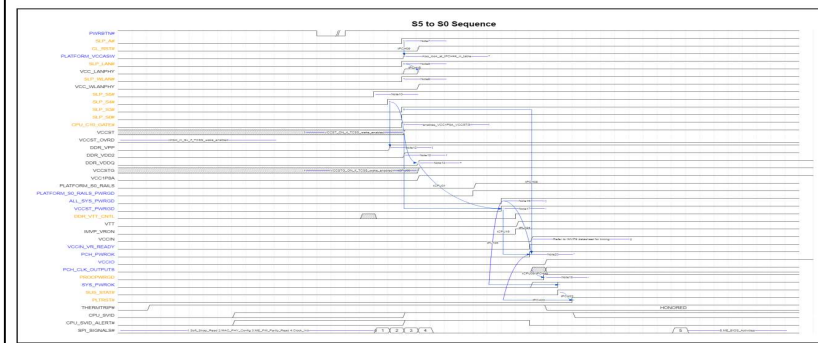
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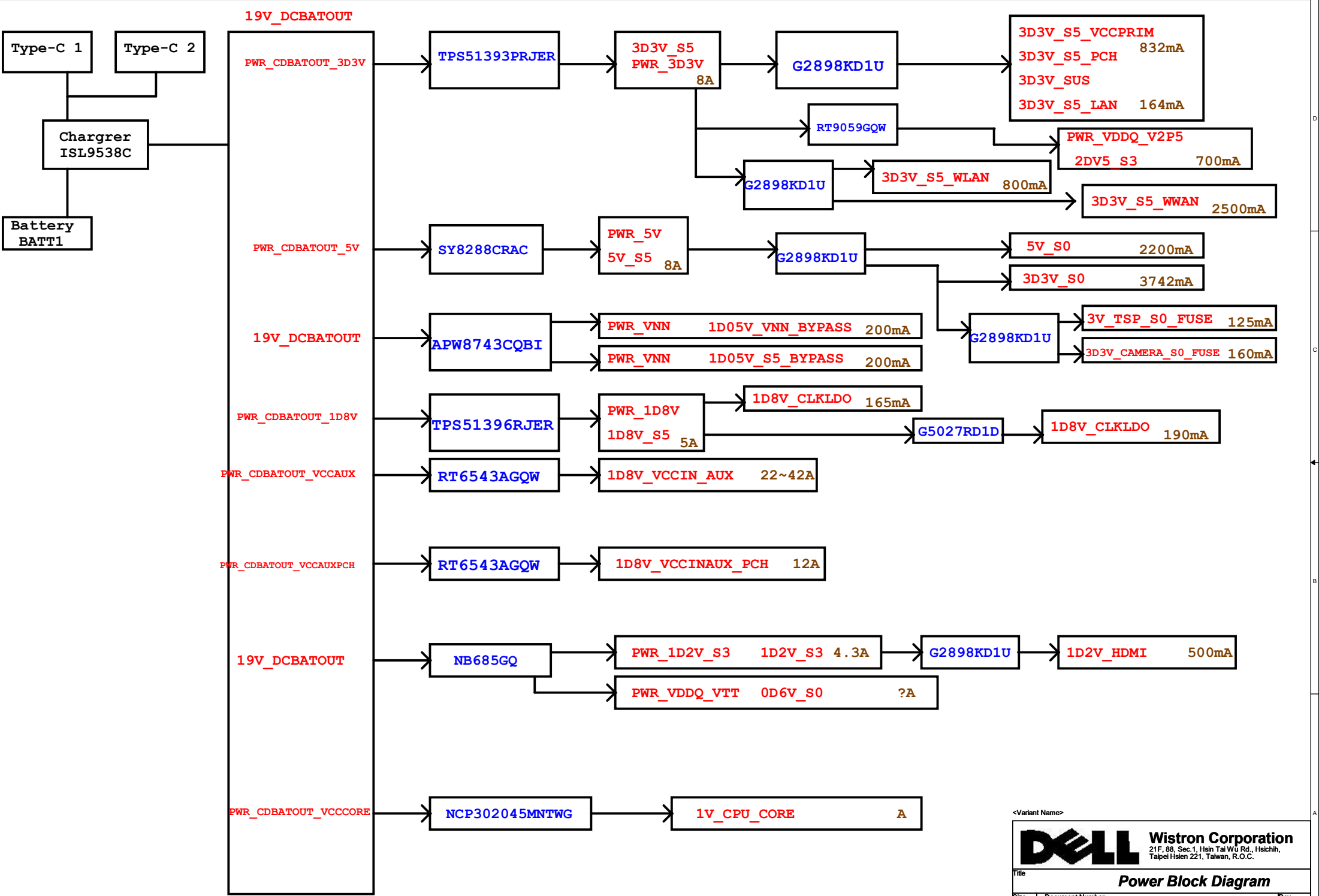
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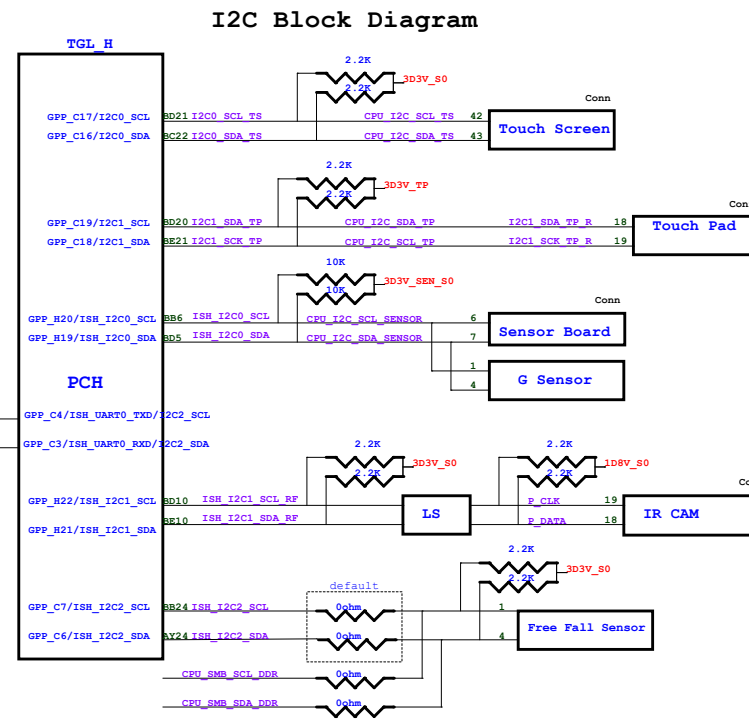
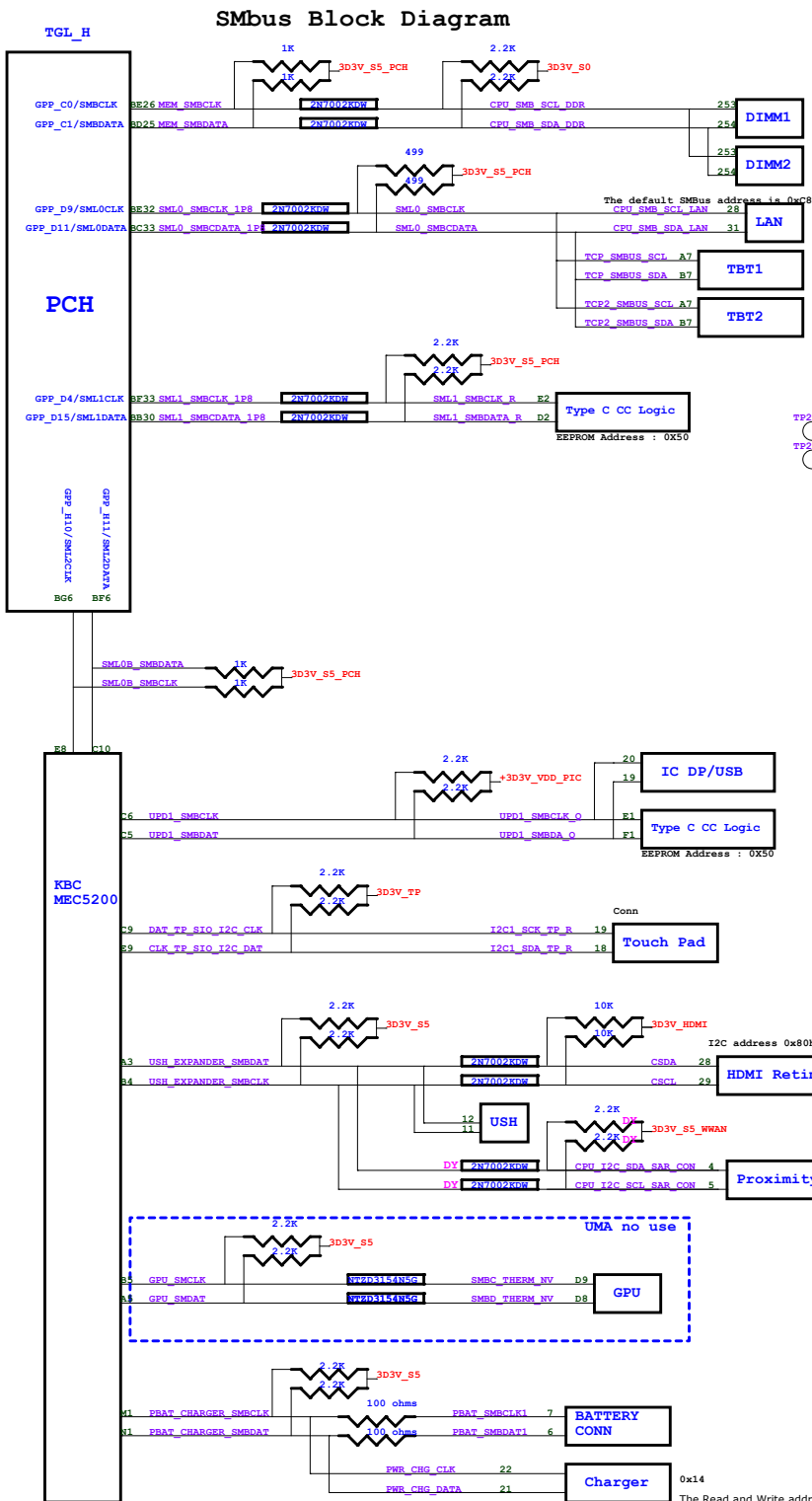


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Change History			
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[illegible]





The I219's address is assigned using SMBus ARP protocol.
The default SMBus address is 0xC8

LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	20	Q/I	B-dr	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 490Ω resistor (write in Sn mode).
SMB_DATA	31	Q/I	B-dr	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 490Ω resistor (write in Sn mode).

Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

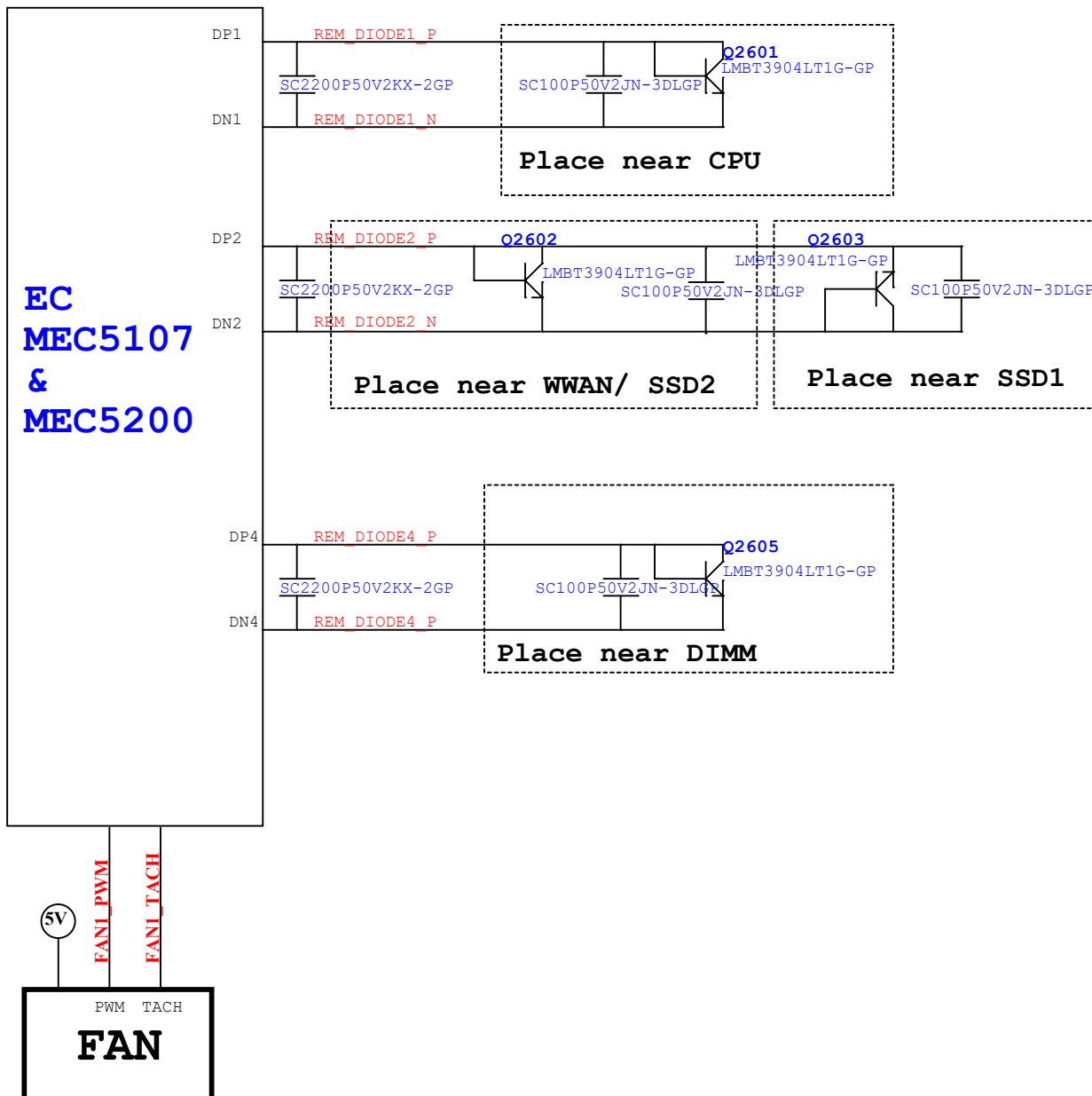
Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings			
Total Bus Capacitance (C _B)	External Pull-up	PCH Pull Down Strength (Refer EDS)	
Up to 400 pF	2.2KΩ	100Ω	
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Resistor Settings			
Total Bus Capacitance (C _B)	External Pull-up	PCH Pull Down Strength	

Up to 100pF	2.7KΩ	100Ω
Up to 200pF	1.5KΩ	
Up to 300pF	1KΩ	
Up to 400 pF	680Ω	
Fast mode Plus (1MRs) - Pull-up/Pull-down strength Settings		
Total Bus Capacitance (C _B)	External Pull-up	PCH Pull Down Strength
Up to 50pF	2.2KΩ	100Ω
Up to 100pF	1.2KΩ	
Up to 200pF	560Ω	
Up to 300pF	390Ω	
Up to 400 pF	270Ω	

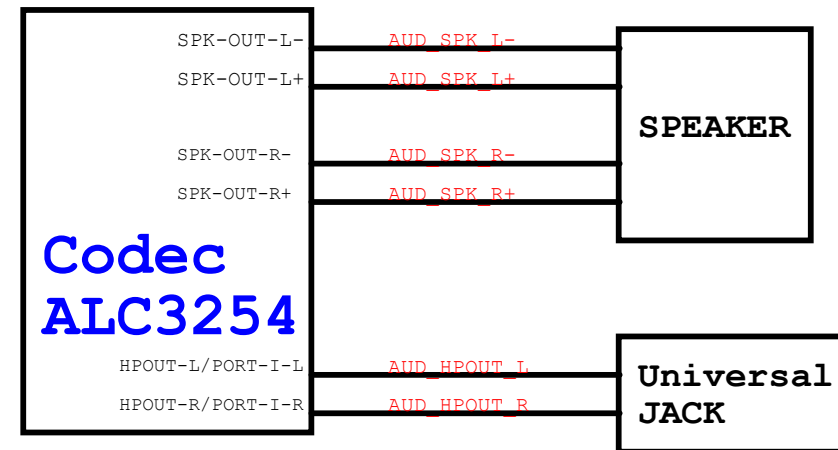
The Read and Write address for the ISL9538C is
 • Read address = 0b00010011 (0X13H)/0b00011011 (0X1BH)
 • Write address = 0b00010010 (0X12H)/0b00011010 (0X1AH)

<Variant Name>

Thermal Block Diagram



Audio Block Diagram



<Variant Name>



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Title

THERMAL/AUDIO BLOCK DIAGRAM

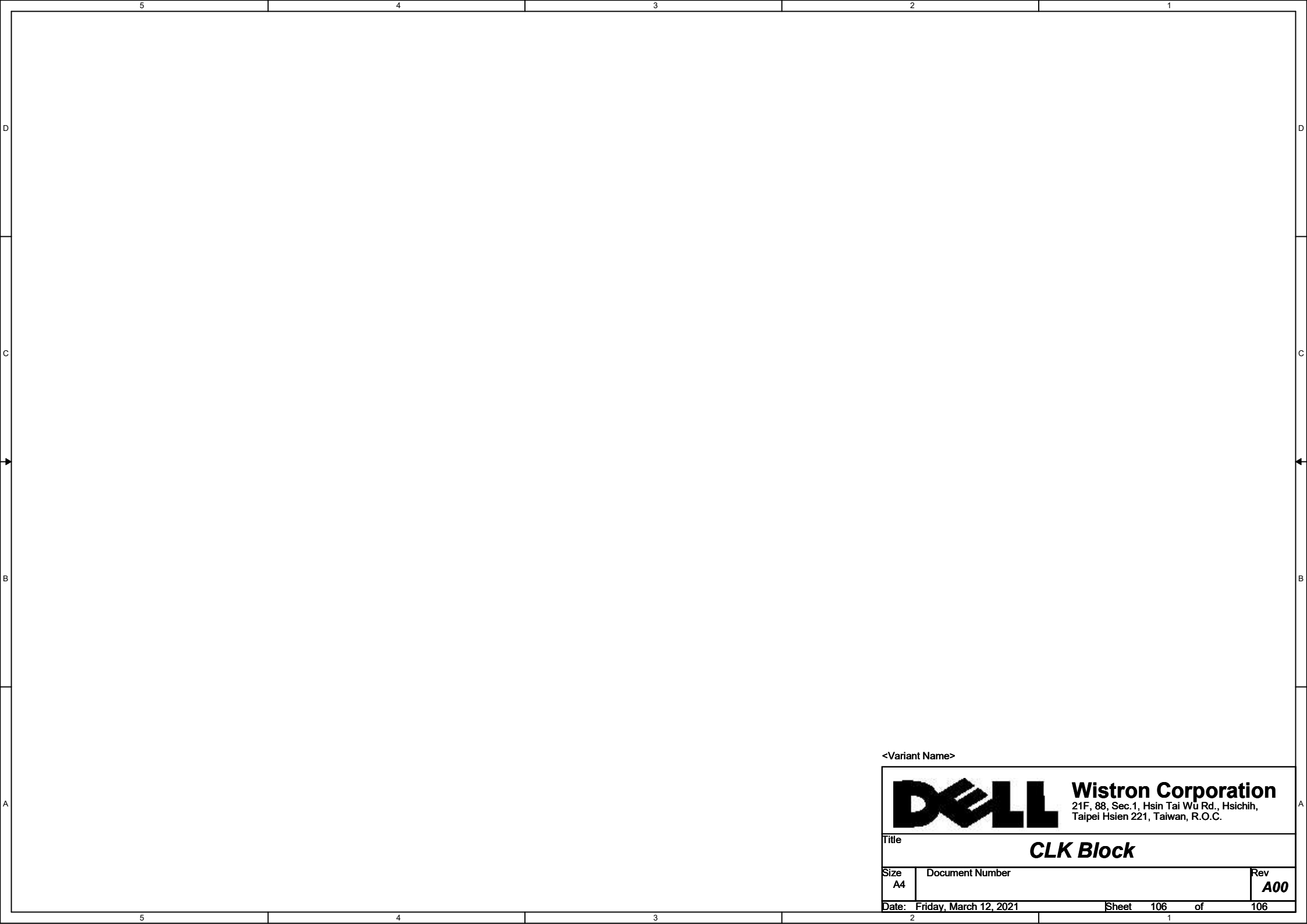
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CLK Block			
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